LMV551/LMV552/LMV554 3 MHz, Micropower RRO Amplifiers

Check for Samples: LMV551, LMV552

FEATURES

- **(Typical 5V Supply, Unless Otherwise Noted.)**
- **Guaranteed 3V and 5.0V Performance**
- **High Unity Gain Bandwidth 3 MHz**
- **Supply Current (Per Amplifier) 37 μA**
- **CMRR 93 dB**
- **PSRR 90 dB**
- **Slew Rate 1 V/μs**
- **Output Swing with 100 kΩ Load 70 mV From Rail**
- **Total Harmonic Distortion 0.003% @ 1 kHz, 2 kΩ**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **Active Filter**
- **Portable Equipment**
- **Automotive**
- **Battery Powered Systems**
- **Sensors and Instrumentation**

DESCRIPTION

The LMV551/LMV552/LMV554 are high performance, low power operational amplifiers implemented with TI's advanced VIP50 process. They feature 3 MHz of bandwidth while consuming only 37 μA of current per amplifier, which is an exceptional bandwidth to power ratio in this op amp class. These amplifiers are unity gain stable and provide an excellent solution for low power applications requiring a wide bandwidth.

The LMV551/LMV552/LMV554 have a rail-to-rail output stage and an input common mode range that extends below ground.

The LMV551/LMV552/LMV554 have an operating supply voltage range from 2.7V to 5.5V. These amplifiers can operate over a wide temperature range (−40°C to 125°C) making them a great choice for automotive applications, sensor applications as well as portable instrumentation applications. The LMV551 is offered in the ultra tiny 5-Pin SC70 and 5-Pin SOT-23 package. The LMV552 is offered in an 8-Pin VSSOP package. The LMV554 is offered in the 14-Pin TSSOP.

Typical Application

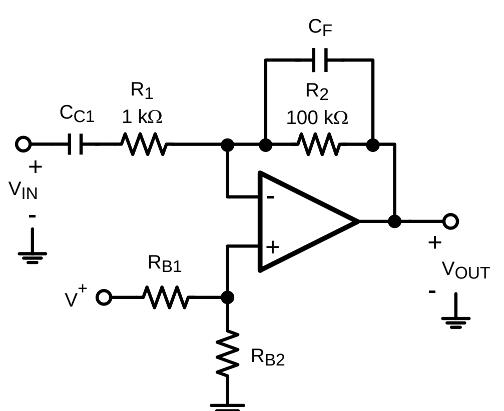

Figure .

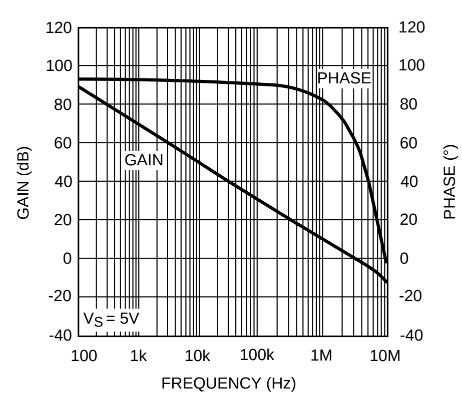

Figure 1. Open Loop Gain and Phase vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

ESD Tolerance [3]	
Human Body Model	
LMV551/LMV552/LMV554	2 KV
Machine Model	
LMV551	100V
LMV552/LMV554	250V
V_{IN} Differential (@ V^+ = 5V)	±2.5V
Supply Voltage (V^+ - V^-)	6V
Voltage at Input/Output pins	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature [4]	150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings [1]

Temperature Range [2]	−40°C to 125°C
Supply Voltage (V^+ – V^-)	2.7V to 5.5V
Package Thermal Resistance (θ_{JA} [2])	
5-Pin SC70	456°C/W
5-Pin SOT-23	234°C/W
8-Pin VSSOP	235°C/W
14-Pin TSSOP	160°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes. [1]

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
V_{OS}	Input Offset Voltage			1	3 **4.5**	mV
TC V_{OS}	Input Offset Average Drift			3.3		µV/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes. [1]

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
I_B	Input Bias Current	[4]			20	38	nA
I_{OS}	Input Offset Current				1	20	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} 2.0V		74 **72**	92		dB
PSRR	Power Supply Rejection Ratio	3.0 ≤ V^+ ≤ 5V, V_{CM} = 0.5V	LMV551/LMV552	80 **78**	92		dB
			LMV554	78 **76**			
		2.7 ≤ V^+ ≤ 5.5V, V_{CM} = 0.5V	LMV551/LMV552	80 **78**	92		
			LMV554	78 **76**			
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 68 dB **CMRR ≥ 60 dB**		0 **0**		2.1 **2.1**	V
A_{VOL}	Large Signal Voltage Gain	0.4 ≤ V_O ≤ 2.6, R_L = 100 kΩ to $V^+/2$	LMV551/LMV552	81 **78**	90		dB
			LMV554	79 **77**			
		0.4 ≤ V_O ≤ 2.6, R_L = 10 kΩ to $V^+/2$		71 **68**	80		
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$			40	48 **58**	mV from rail
		R_L = 10 kΩ to $V^+/2$			85	100 **120**	
	Output Swing Low	R_L = 100 kΩ to $V^+/2$			50	65 **77**	
		R_L = 10 kΩ to $V^+/2$			95	110 **130**	
I_{SC}	Output Short Circuit Current	Sourcing [5]			10		mA
		Sinking [5]			25		
I_S	Supply Current per Amplifier				34	42 **52**	μA
SR	Slew Rate	A_V = +1, 10% to 90% [6]			1		V/μs
Φm	Phase Margin	R_L = 10 kΩ, C_L = 20 pF			75		Deg
GBW	Gain Bandwidth Product				3		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz			70		$nV/\sqrt{Hz}$
		f = 1 kHz			70		
i_n	Input-Referred Current Noise	f = 100 kHz			0.1		$pA/\sqrt{Hz}$
		f = 1 kHz			0.15		
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.003		%

(4) Positive current corresponds to current flowing into the device.
(5) The part is not short circuit protected and is not recommended for operation with heavy resistive loads.
(6) Slew rate is the average of the rising and falling slew rates.

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [1]	Typ [2]	Max [1]	Units
V_{OS}	Input Offset Voltage			1	3.0 **4.5**	mV
TC V_{OS}	Input Offset Average Drift			3.3		μV/°C
I_B	Input Bias Current	[3]		20	38	nA
I_{OS}	Input Offset Current			1	20	nA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 4.0V	76 **74**	93		dB
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V to V_{CM} = 0.5V	78 **75**	90		dB
		2.7V ≤ V^+ ≤ 5.5V to V_{CM} = 0.5V	78 **75**	90		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 68 dB CMRR ≥ 60 dB	0 **0**		4.1 **4.1**	V
A_{VOL}	Large Signal Voltage Gain	0.4 ≤ V_O ≤ 4.6, R_L = 100 kΩ to $V^+/2$	78 **75**	90		dB
		0.4 ≤ V_O ≤ 4.6, R_L = 10 kΩ to $V^+/2$	75 **72**	80		
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$		70	92 **122**	mV from rail
		R_L = 10 kΩ to $V^+/2$		125	155 **210**	
	Output Swing Low	R_L = 100 kΩ to $V^+/2$		60	70 **82**	
		R_L = 10 kΩ to $V^+/2$		110	130 **155**	
I_{SC}	Output Short Circuit Current	Sourcing [4]		10		mA
		Sinking [4]		25		
I_S	Supply Current Per Amplifier			37	46 **54**	μA
SR	Slew Rate	A_V = +1, V_O = 1 V_{PP} 10% to 90% [5]		1		V/μs
Φm	Phase Margin	R_L = 10 kΩ, C_L = 20 pF		75		Deg
GBW	Gain Bandwidth Product			3		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		70		$nV/\sqrt{Hz}$
		f = 1 kHz		70		
i_n	Input-Referred Current Noise	f = 100 kHz		0.1		$pA/\sqrt{Hz}$
		f = 1 kHz		0.15		
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.003		%

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short circuit protected and is not recommended for operation with heavy resistive loads.
(5) Slew rate is the average of the rising and falling slew rates.

CONNECTION DIAGRAM

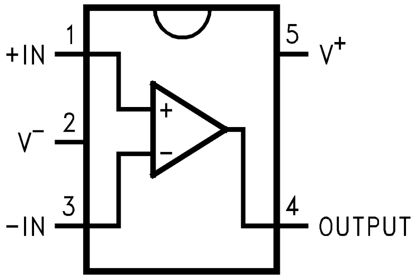

Figure 2. 5-Pin SC70/ SOT-23 Top View

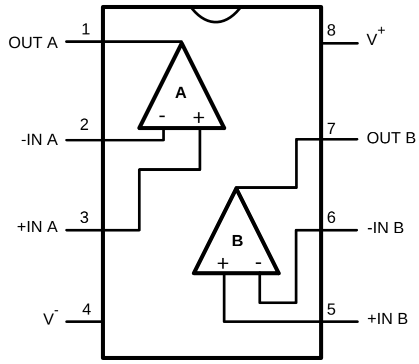

Figure 3. 8-Pin VSSOP Top View

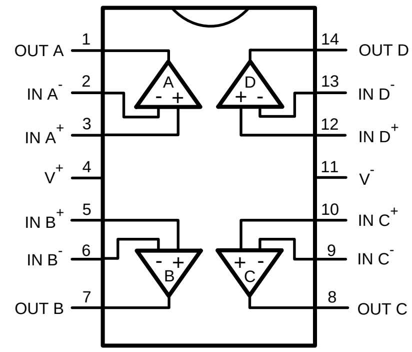

Figure 4. 14-Pin TSSOP Top View

TYPICAL CHARACTERISTICS

Open Loop Gain and Phase with Capacitive Load

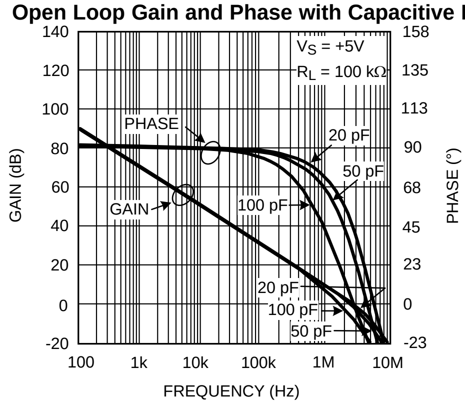

Figure 5.

Open Loop Gain and Phase with Resistive Load

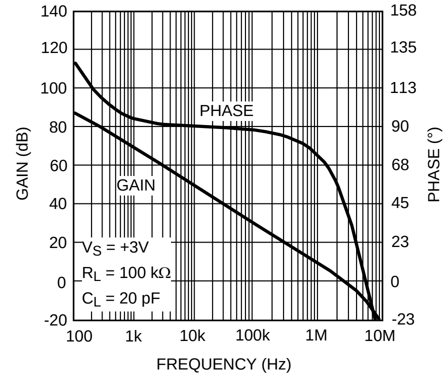

Figure 6.

Open Loop Gain and Phase with Resistive Load

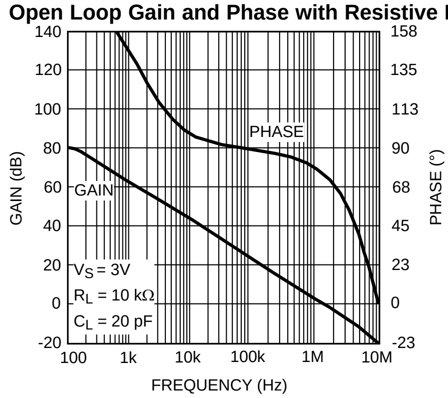

Figure 7.

Open Loop Gain and Phase with Resistive Load

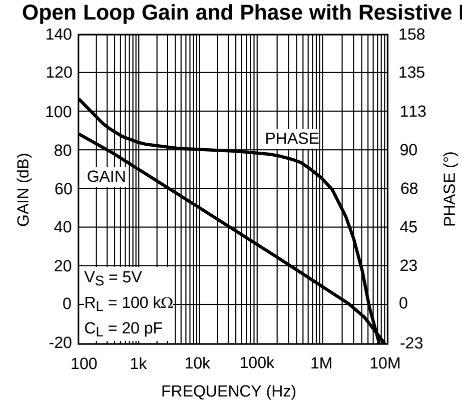

Figure 8.

Open Loop Gain and Phase with Resistive Load

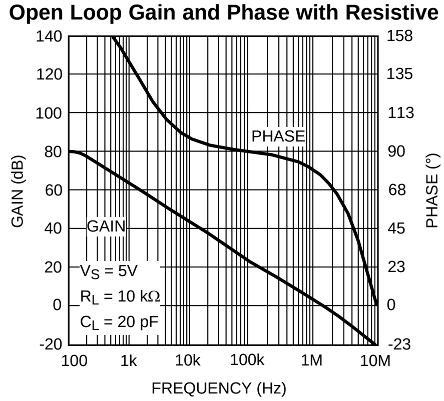

Figure 9.

Slew Rate vs. Supply voltage

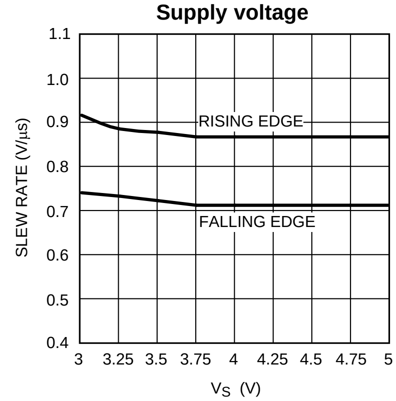

Figure 10.

TYPICAL CHARACTERISTICS (continued)

Small Signal Transient Response

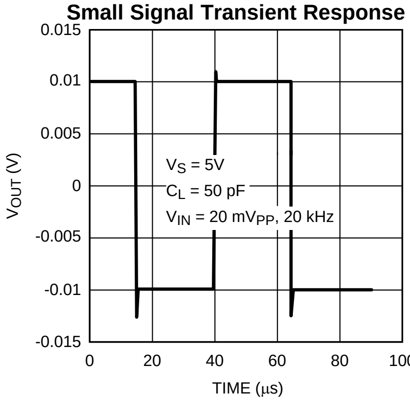

Figure 11.

Large Signal Transient Response

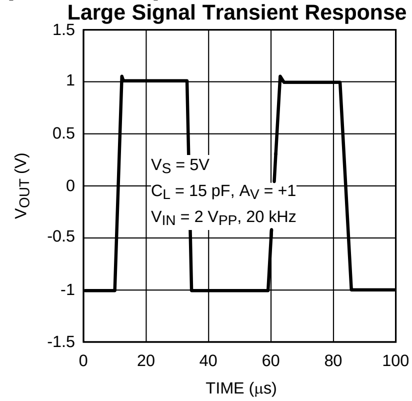

Figure 12.

Small Signal Transient Response

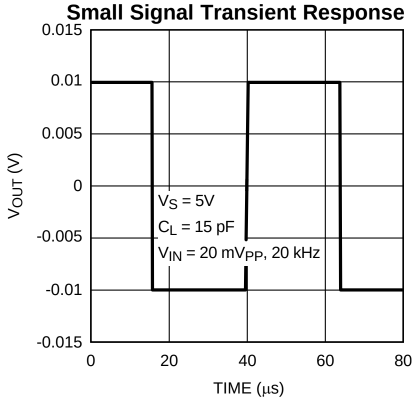

Figure 13.

Input Referred Noise vs. Frequency

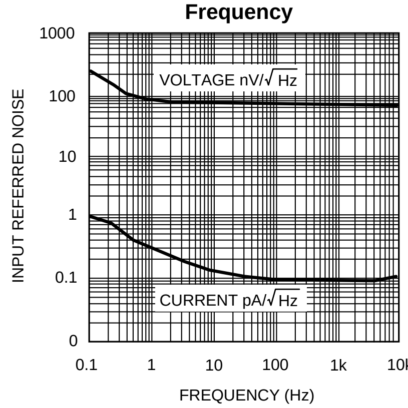

Figure 14.

THD+N vs. Amplitude @ 3V

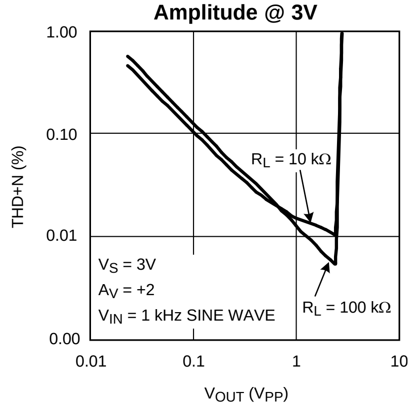

Figure 15.

THD+N vs. Amplitude @ 5V

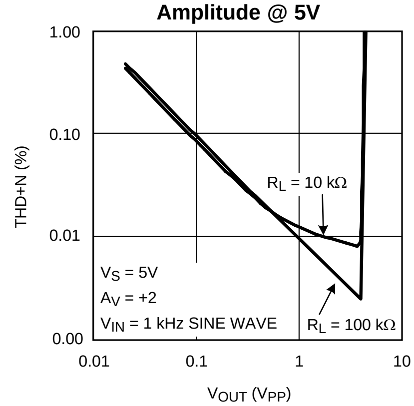

Figure 16.

TYPICAL CHARACTERISTICS (continued)

THD+N vs. Amplitude

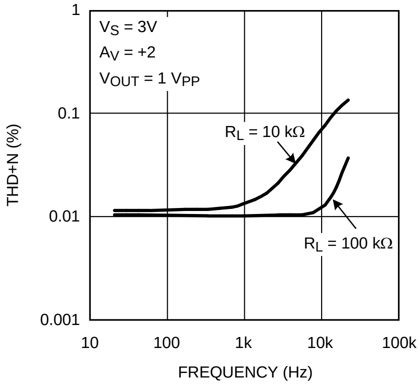

Figure 17.

THD+N vs. Amplitude

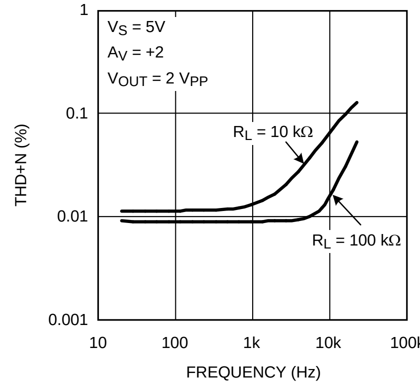

Figure 18.

Supply Current vs. Supply Voltage

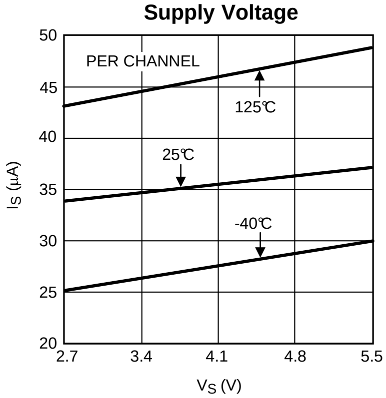

Figure 19.

V_{OS} vs. V_{CM}

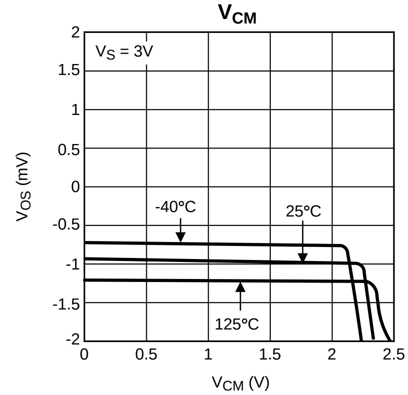

Figure 20.

V_{OS} vs. V_{CM}

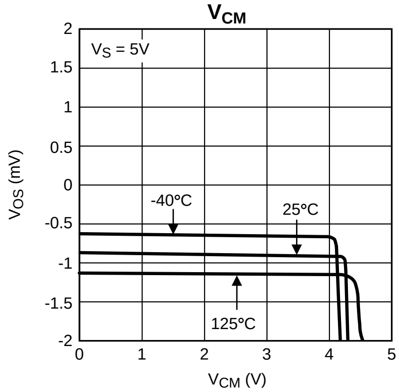

Figure 21.

V_{OS} vs. Supply Voltage

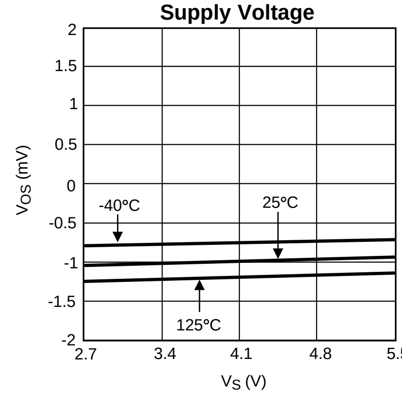

Figure 22.

TYPICAL CHARACTERISTICS (continued)

I_{BIAS} vs. V_{CM}

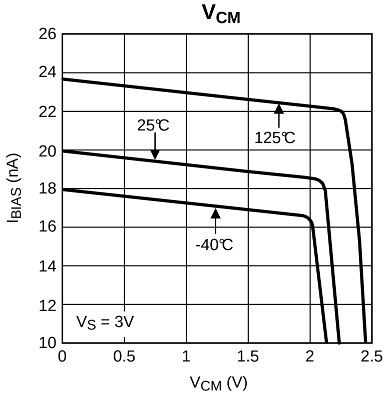

Figure 23.

I_{BIAS} vs. V_{CM}

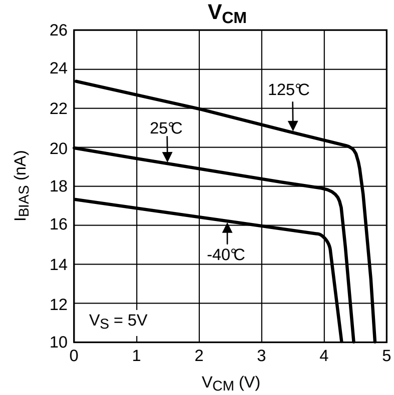

Figure 24.

I_{BIAS} vs. Supply Voltage

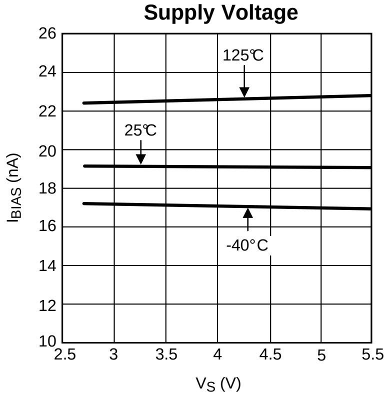

Figure 25.

Positive Output Swing vs. Supply Voltage

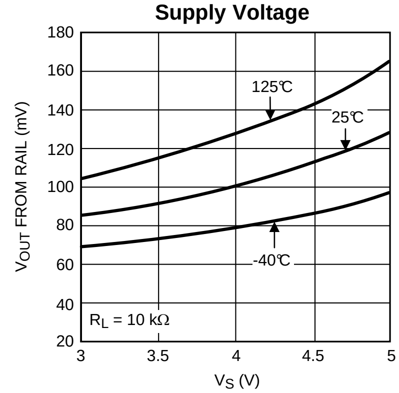

Figure 26.

Negative Output Swing vs. Supply Voltage

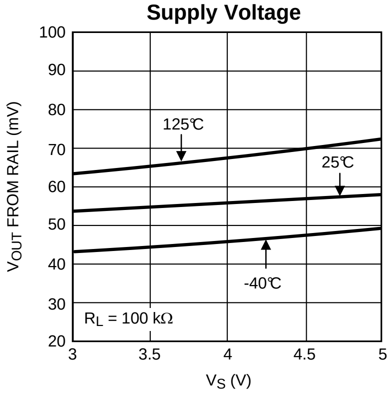

Figure 27.

Positive Output Swing vs. Supply Voltage

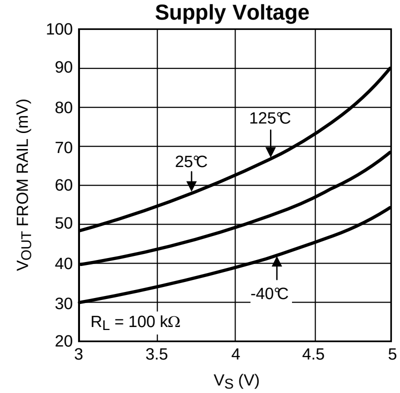

Figure 28.

TYPICAL CHARACTERISTICS (continued)

Negative Output Swing vs. Supply Voltage

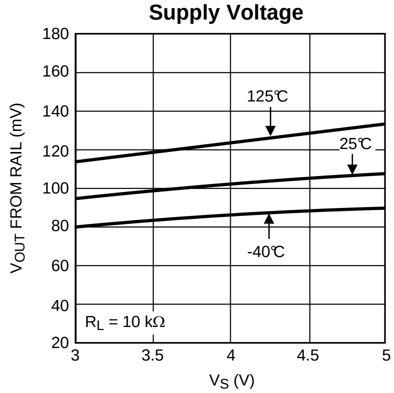

Figure 29.

APPLICATIONS INFORMATION

ADVANTAGES OF THE LMV551/LMV552/LMV554

Low Voltage and Low Power Operation

The LMV551/LMV552/LMV554 have performance guaranteed at supply voltages of 3V and 5V and are guaranteed to be operational at all supply voltages between 2.7V and 5.5V. For this supply voltage range, the LMV551/LMV552/LMV554 draw the extremely low supply current of less than 37 µA per amp.

Wide Bandwidth

The bandwidth to power ratio of 3 MHz to 37 µA per amplifier is one of the best bandwidth to power ratios ever achieved. This makes these devices ideal for low power signal processing applications such as portable media players and instrumentation.

Low Input Referred Noise

The LMV551/LMV552/LMV554 provide a flatband input referred voltage noise density of 70 nV/$\sqrt{Hz}$, which is significantly better than the noise performance expected from an ultra low power op amp. They also feature the exceptionally low 1/f noise corner frequency of 4 Hz. This noise specification makes the LMV551/LMV552/LMV554 ideal for low power applications such as PDAs and portable sensors.

Ground Sensing and Rail-to-Rail Output

The LMV551/LMV552/LMV554 each have a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common mode range includes the negative supply rail which allows direct sensing at ground in a single supply operation.

Small Size

The small footprints of the LMV551/LMV552/LMV554 packages save space on printed circuit boards, and enable the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, the amplifiers can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity

STABILITY OF OP AMP CIRCUITS

Stability and Capacitive Loading

As seen in the Phase Margin vs. Capacitive Load graph, the phase margin reduces significantly for C_L greater than 100 pF. This is because the op amp is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing them for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth of the op amp. Hence, if the LMV551/LMV552/LMV554 are to be used for driving higher capacitive loads, they will have to be externally compensated.

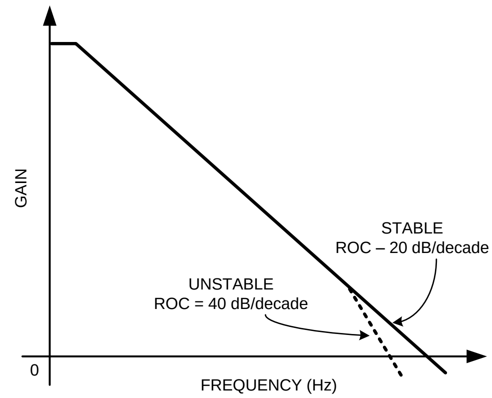

Figure 30. Gain vs. Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC, which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the op amp's unity gain bandwidth, the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 30). This increases the ROC to 40 dB/ decade and causes instability.

In such a case a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

In the Loop Compensation

Figure 31 illustrates a compensation technique, known as 'in the loop' compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

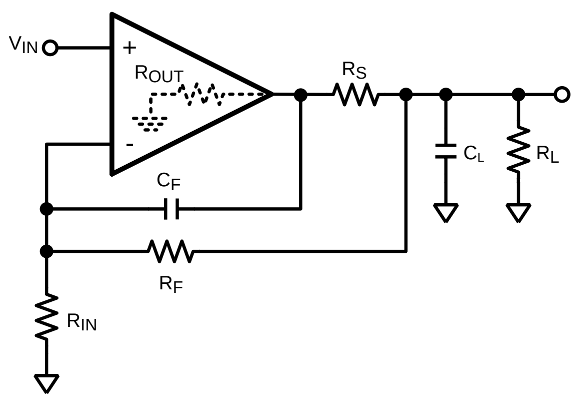

Figure 31. In the Loop Compensation

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown in Figure 31 the values of R_S and C_F are given by Equation 1. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F, R_{IN}, and R_L are to be 10 kΩ, while R_{OUT} is 340Ω.

$$R_S = \frac{R_{OUT} R_{IN}}{R_F}$$

$$C_F = \left(1 + \frac{1}{A_{CL}}\right)\left(\frac{R_F + 2R_{IN}}{R_F^2}\right) C_L R_{OUT} \quad (1)$$

Table 1. Phase Margins

C_L (pF)	R_S (Ω)	C_F (pF)	Phase Margin (°)
50	340	8	47
100	340	15	42
150	340	22	40

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_F and C_F.

Compensation by External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 32. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with less ringing and overshoot, but will also limit the output swing and the short circuit current of the circuit.

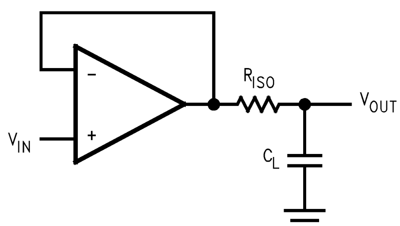

Figure 32. Compensation by Isolation Resistor

TYPICAL APPLICATION

ACTIVE FILTERS

With a wide unity gain bandwidth of 3 MHz, low input referred noise density and a low power supply current, the LMV551/LMV552/LMV554 are well suited for low-power filtering applications. Active filter topologies, such as the Sallen-Key low pass filter shown in Figure 33, are very versatile, and can be used to design a wide variety of filters (Chebyshev, Butterworth or Bessel). The Sallen-Key topology, in particular, can be used to attain a wide range of Q, by using positive feedback to reject the undesired frequency range.

In the circuit shown in Figure 33, the two capacitors appear as open circuits at lower frequencies and the signal is simply buffered to the output. At high frequencies the capacitors appear as short circuits and the signal is shunted to ground by one of the capacitors before it can be amplified. Near the cut-off frequency, where the impedance of the capacitances is on the same order as R_G and R_F, positive feedback through the other capacitor allows the circuit to attain the desired Q.

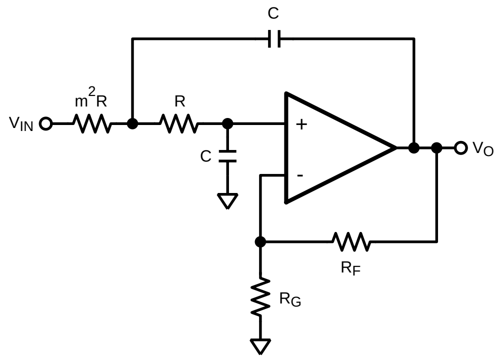

Figure 33. Sallen-Key Filter

REVISION HISTORY

Changes from Revision F (February 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV551MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF3A	Samples
LMV551MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF3A	Samples
LMV551MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A94	Samples
LMV551MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A94	Samples
LMV552MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH3A	Samples
LMV552MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH3A	Samples
LMV554MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV55 4MT	Samples
LMV554MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV55 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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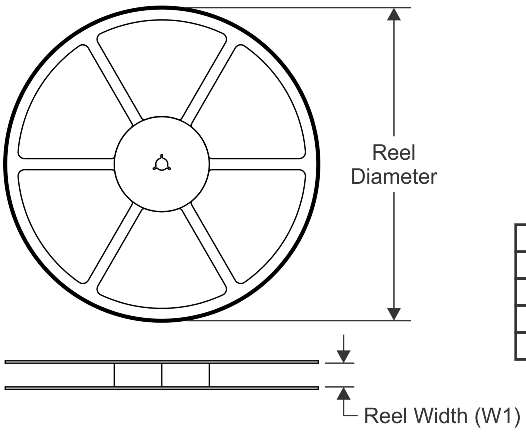
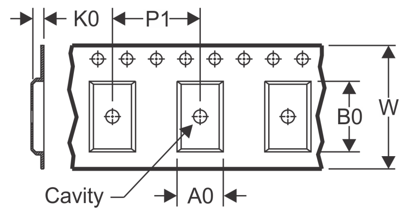
TAPE AND REEL INFORMATION

REEL DIMENSIONS

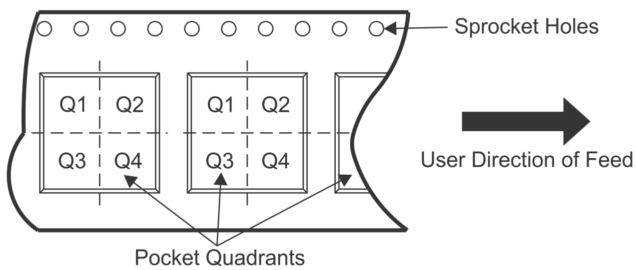


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

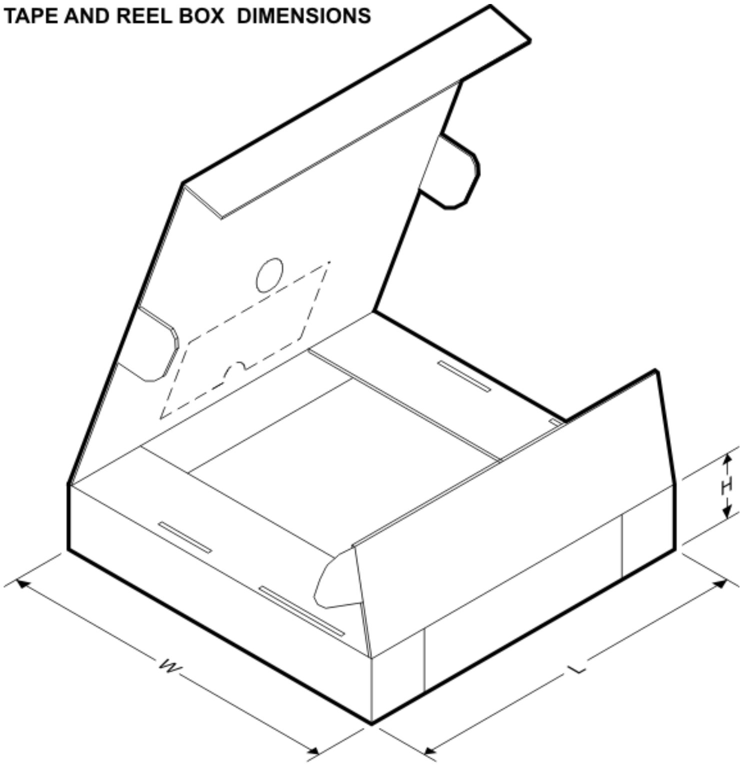
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV551MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV551MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV551MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV551MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV552MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV552MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV554MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

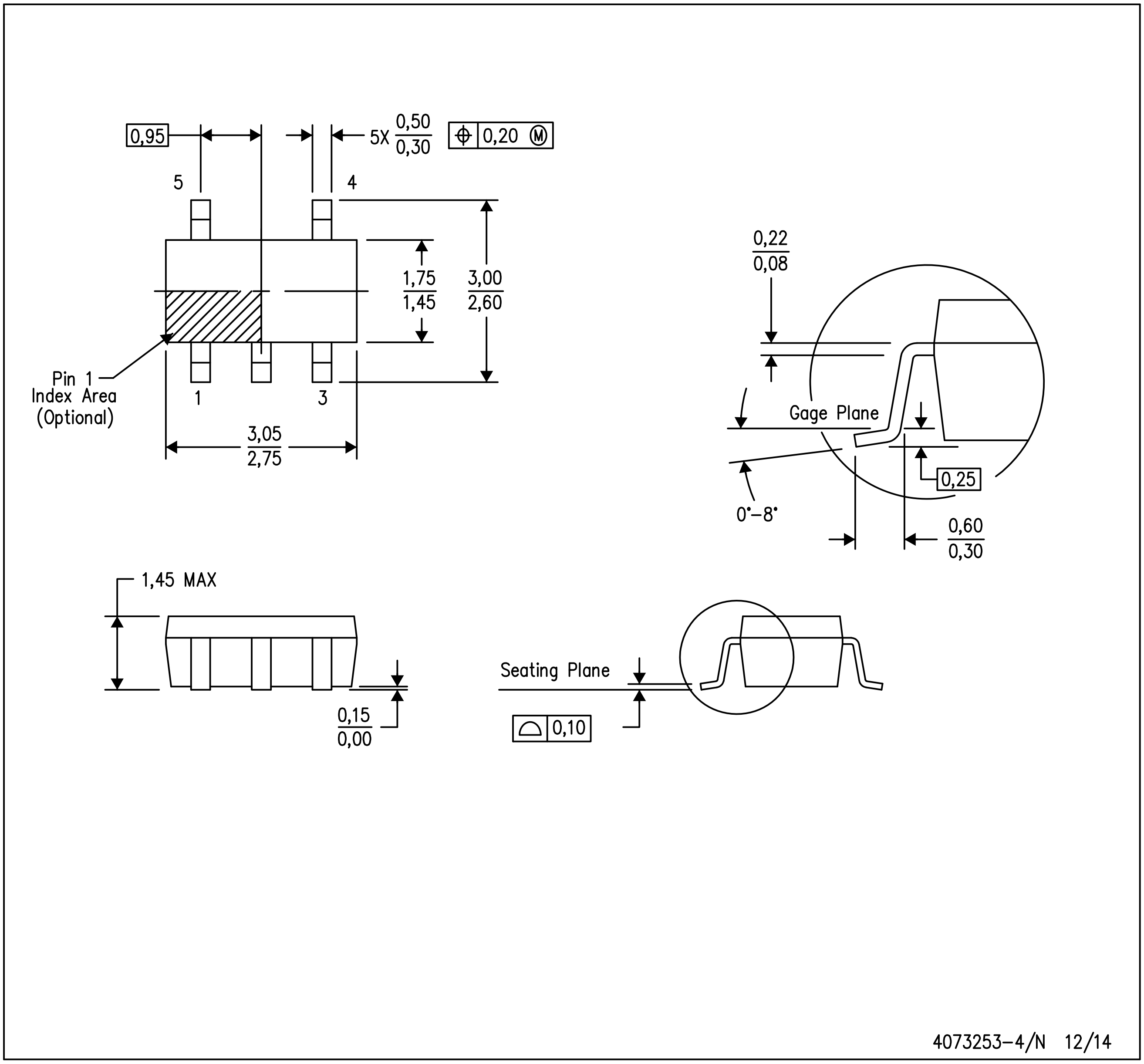
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

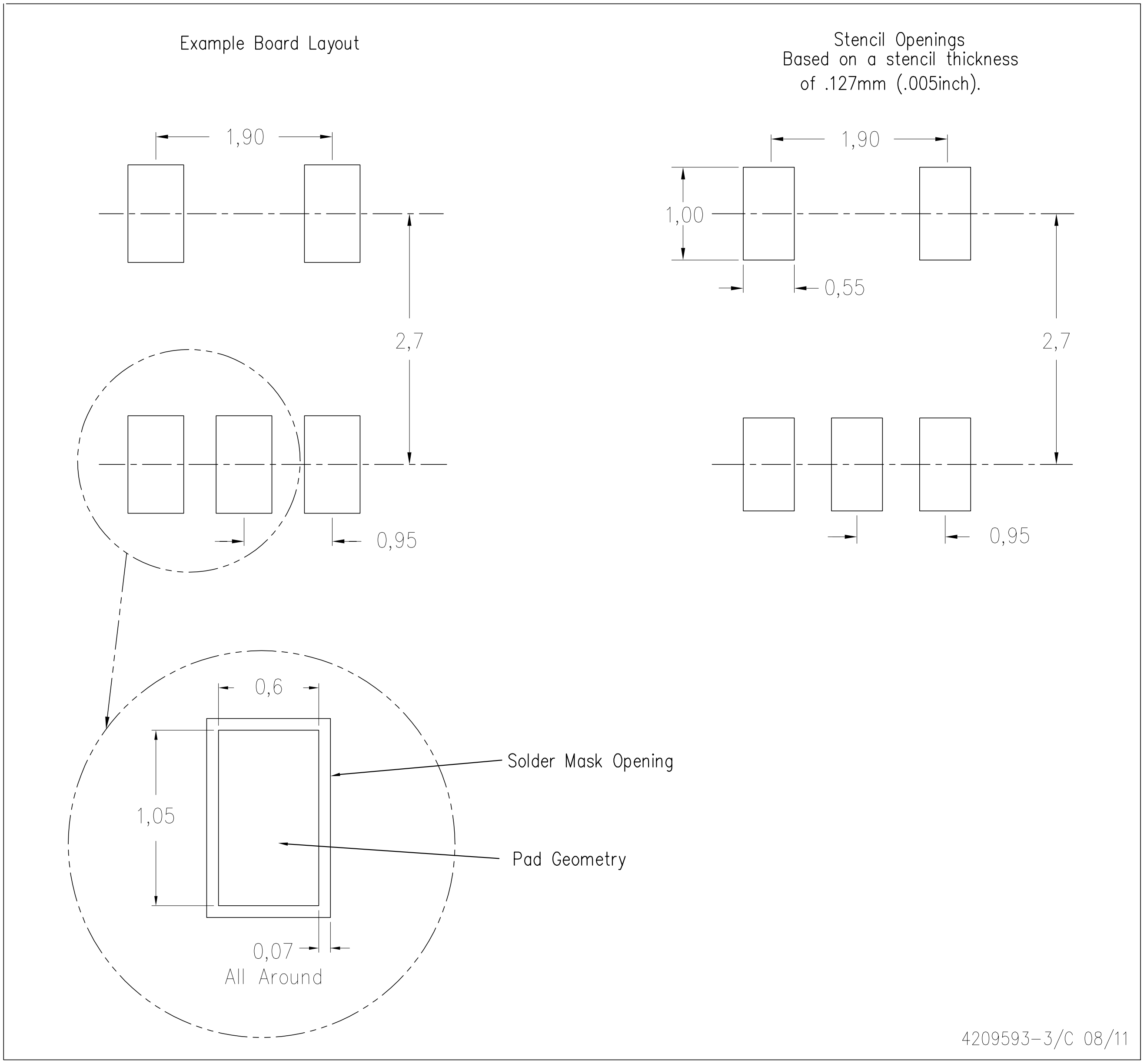
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV551MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV551MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV551MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV551MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV552MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV552MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV554MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



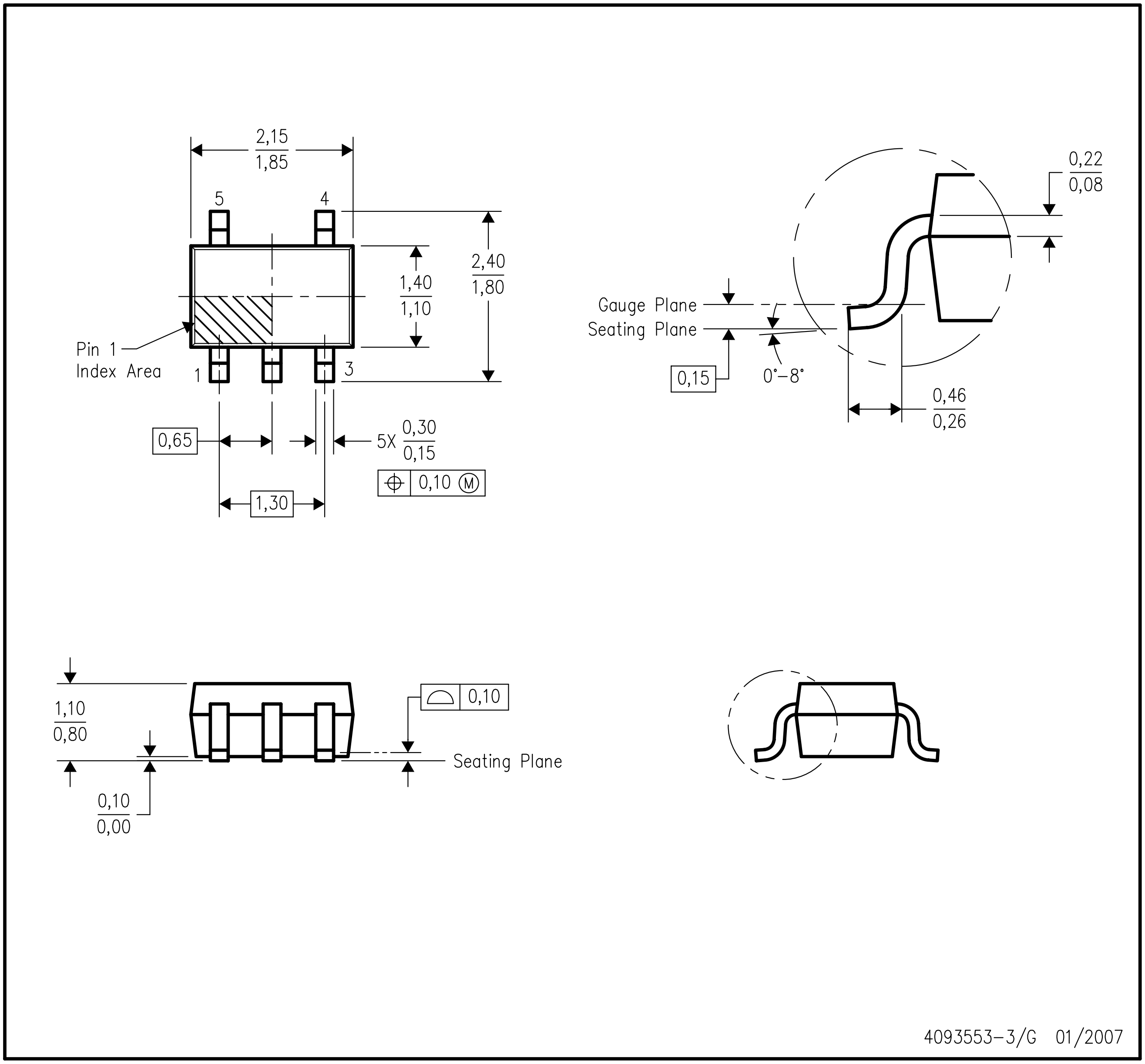
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



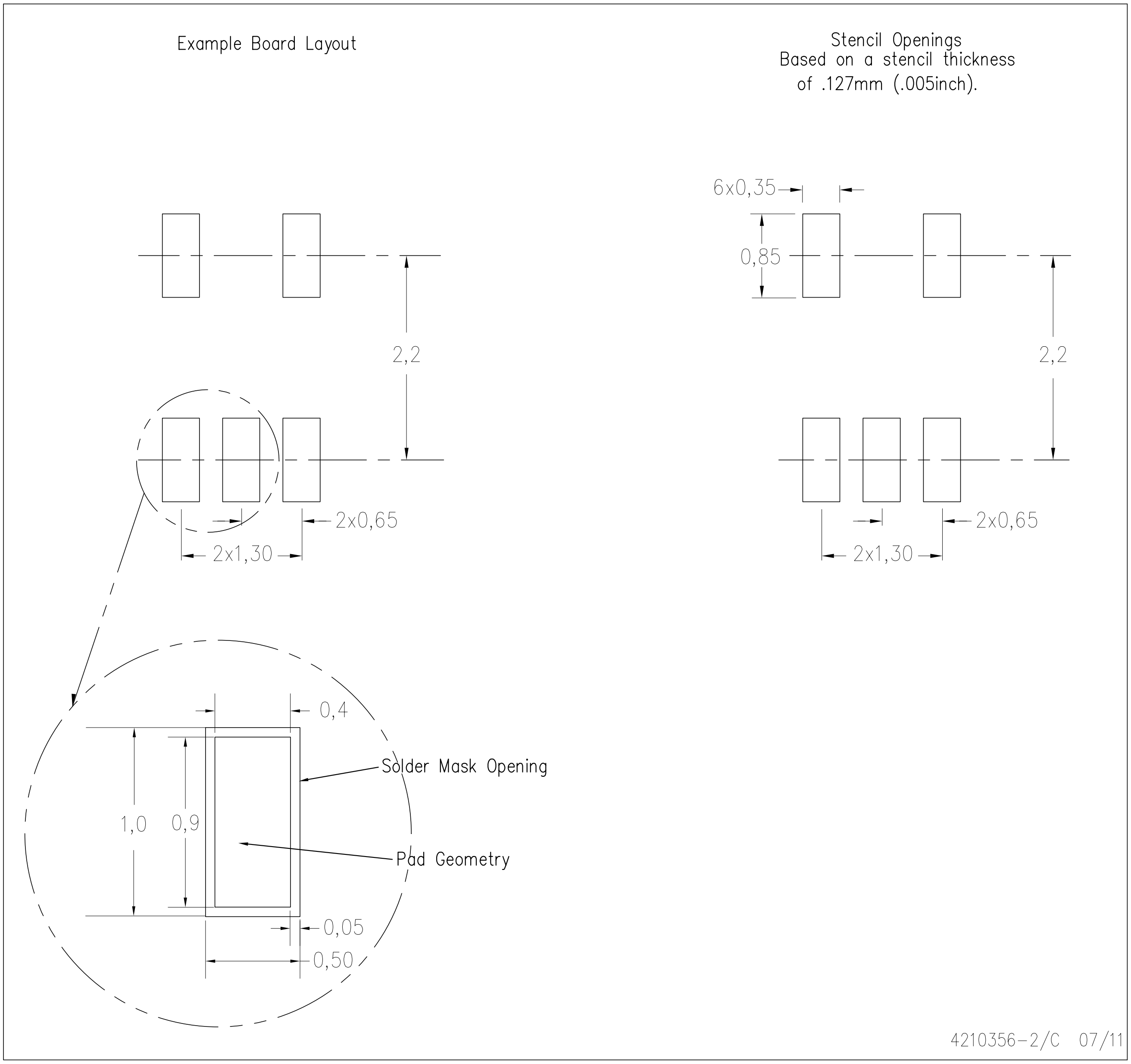
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



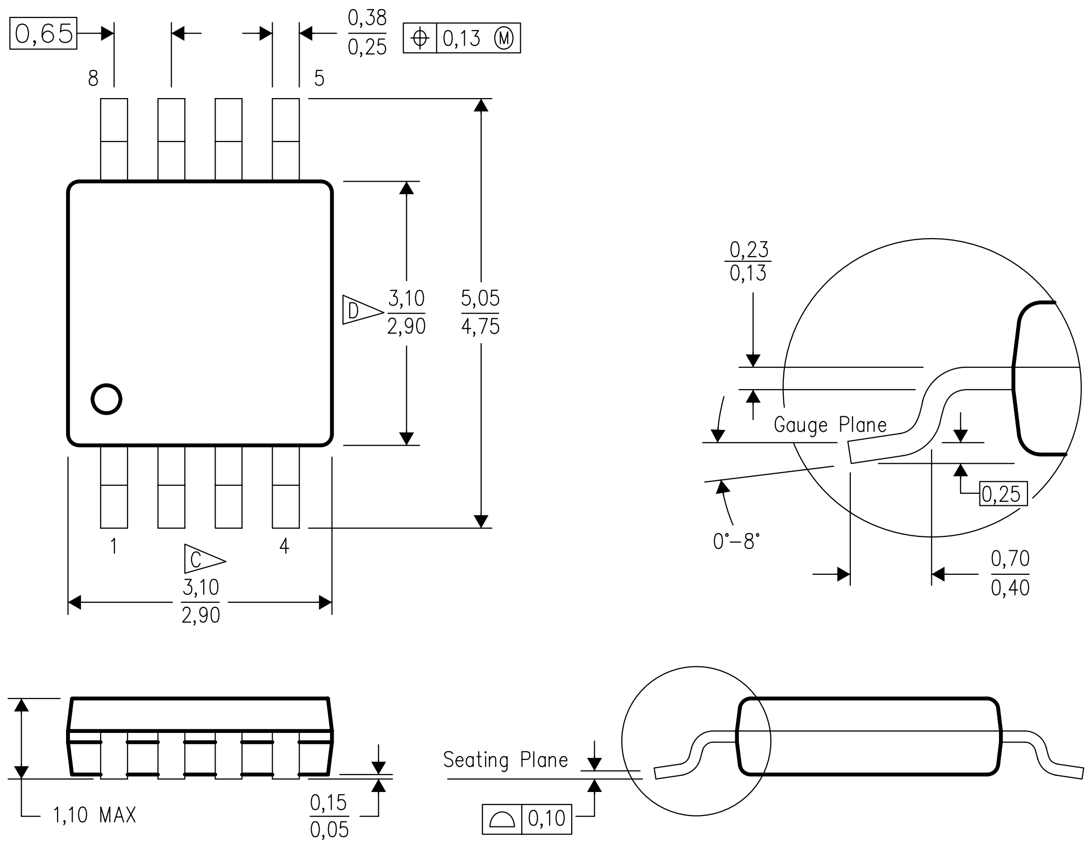
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



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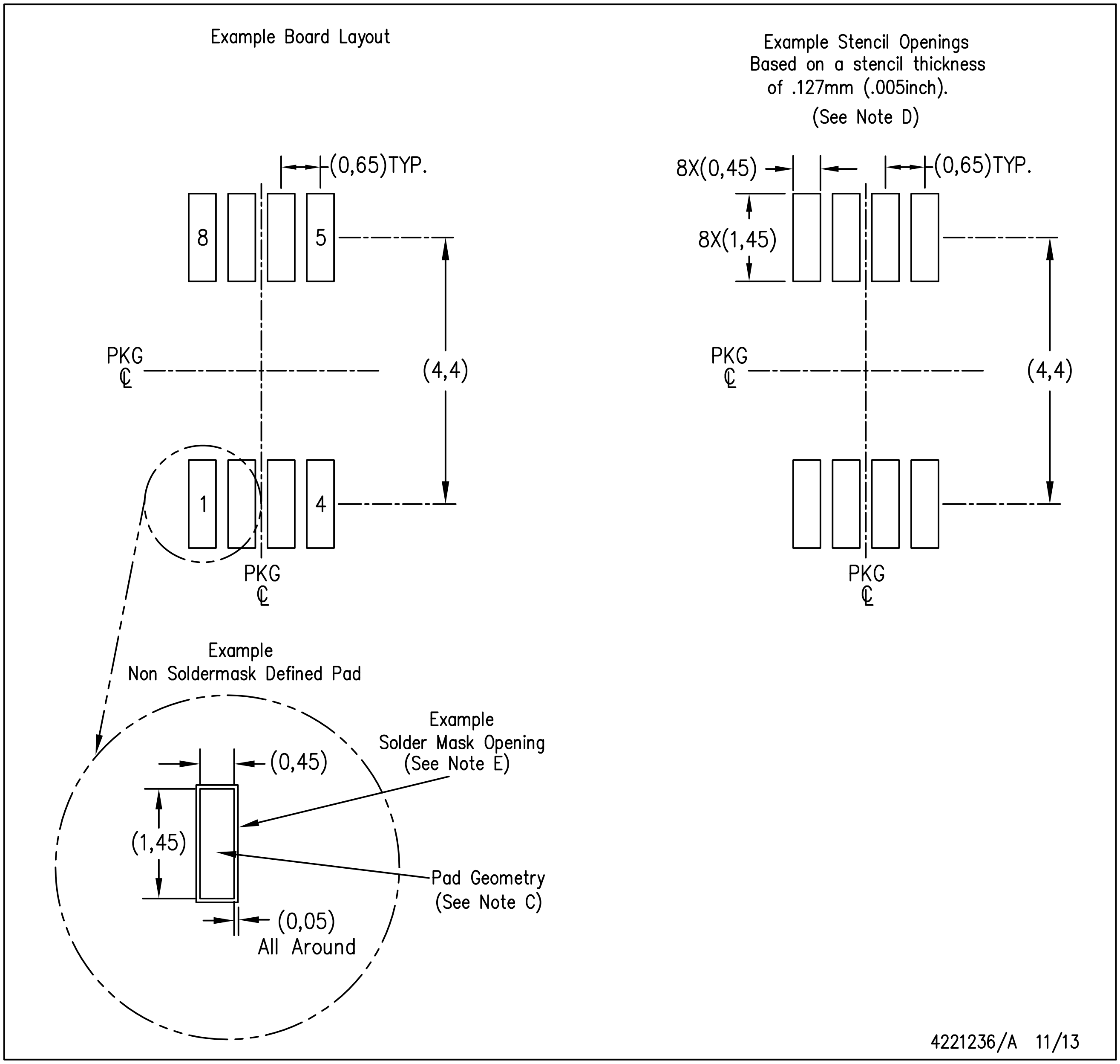
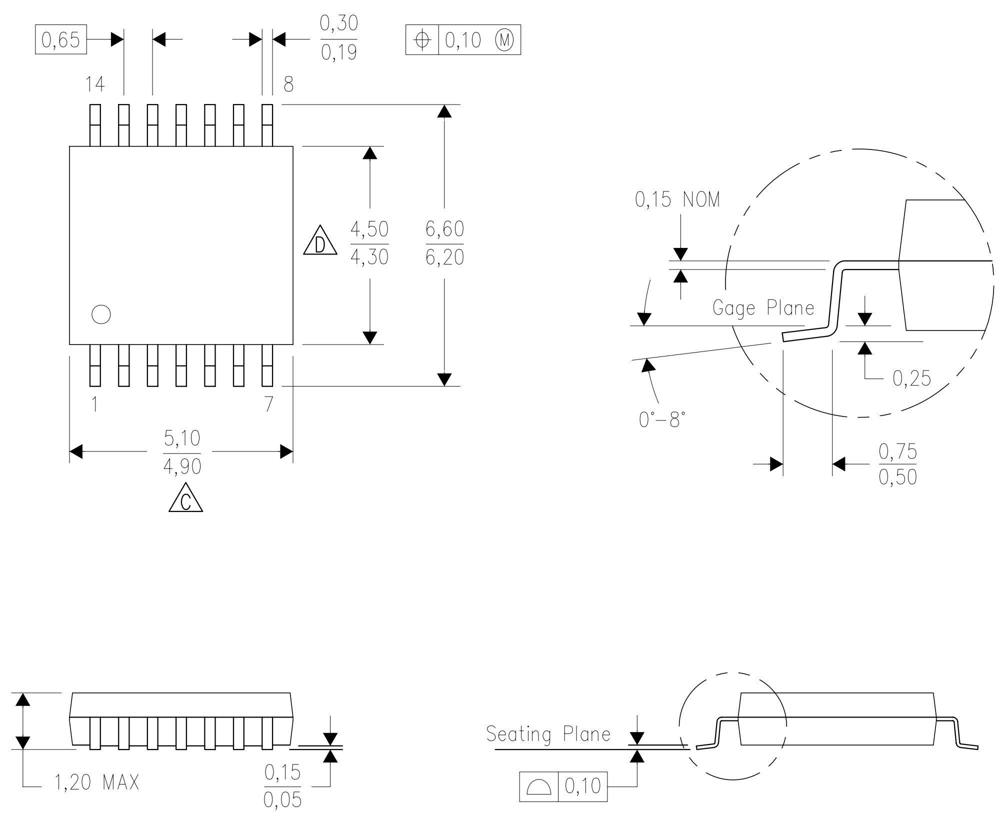
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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