LM3046 Transistor Array

Check for Samples: LM3046

FEATURES

- **Two Matched Pairs of Transistors**
  - **V_{BE} Matched ±5 mV**
  - **Input Offset Current 2 µA Max at I_C = 1 mA**
- **Five General Purpose Monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide Operating Current Range**
- **Low Noise Figure: 3.2 dB typ at 1 kHz**

APPLICATIONS

- **General Use in All Types of Signal Processing Systems Operating Anywhere in the Frequency Range from DC to VHF**
- **Custom Designed Differential Amplifiers**
- **Temperature Compensated Amplifiers**

DESCRIPTION

The LM3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3046 is supplied in a 14-lead SOIC package.

Schematic and Connection Diagram

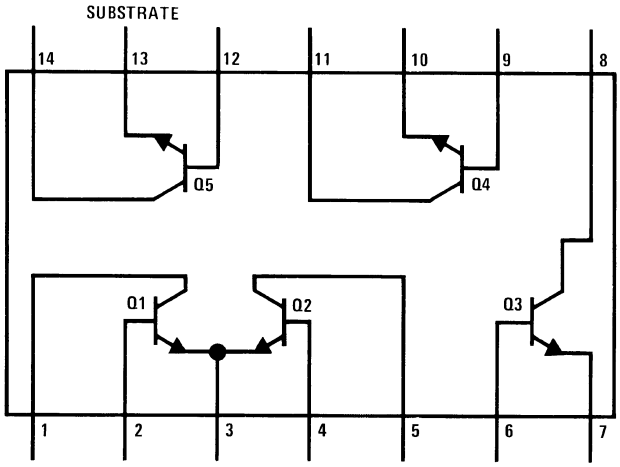

Figure 1. SOIC Package
Top View
See Package Number D (R-PDSO-G14)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

		Each Transistor	Total Package	Units
Power Dissipation	T_A = 25°C	300	750	mW
	T_A = 25°C to 55°C	300	750	
	T_A > 55°C	Derate at 6.67		mW/°C
	T_A = 25°C to 75°C			mW
	T_A > 75°C			mW/°C
Collector to Emitter Voltage, V_{CEO}		15		V
Collector to Base Voltage, V_{CBO}		20		
Collector to Substrate Voltage, V_{CIO}[4]		20		
Emitter to Base Voltage, V_{EBO}		5		
Collector Current, I_C		50		mA
Operating Temperature Range		−40°C to +85°C		
Storage Temperature Range		−65°C to +85°C		
Soldering Information	Dual-In-Line Package Soldering (10 Sec.)	260°C		
	SOIC Package			
	Vapor Phase (60 Seconds)	215°C		
	Infrared (15 Seconds)	220°C		

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.
(2) See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The collector of each transistor is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics(1)

Parameter	Conditions	Min	Typ	Max	Units
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 µA, I_E = 0	20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 µA, I_{CI} = 0	20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 µA, I_C = 0	5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5	µA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V I_C = 10 mA		100		
	I_C = 1 mA	40	100		
	I_C = 10 µA		54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{IO2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2	µA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V I_E = 1 mA		0.715		V
	I_E = 10 mA		0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4}\rvert$, $\lvert V_{BE4} - V_{BE5}\rvert$, $\lvert V_{BE5} - V_{BE3}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5	mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$ (1)	V_{CE} = 3V, I_C = 1 mA		−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$ (2)	V_{CE} = 3V, I_C = 1 mA		1.1		µV/°C
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 µA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		µmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3+J 0.04		
Output Admittance (Y_{oe})			0.001+j 0.03		
Reverse Transfer Admittance (Y_{re})			See Figure 16		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

(1) (T_A = 25°C unless otherwise specified)

Typical Performance Characteristics

Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor

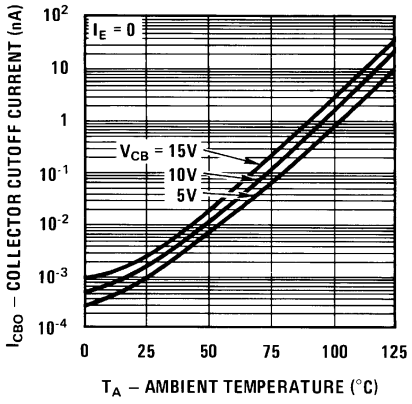

Figure 2.

Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

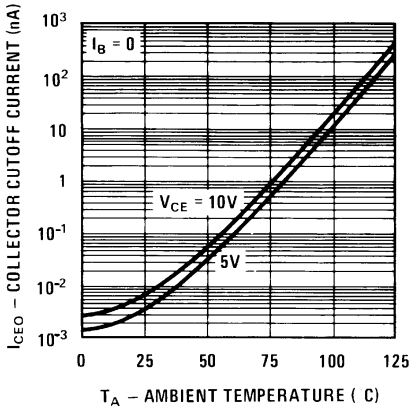

Figure 3.

Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current

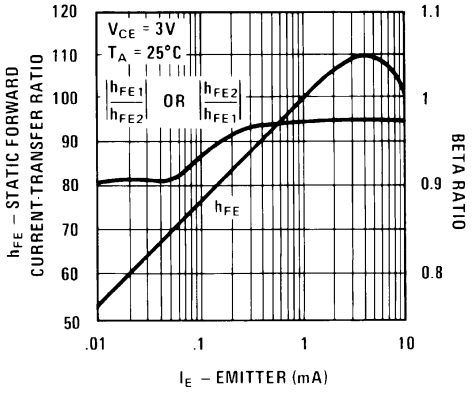

Figure 4.

Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current

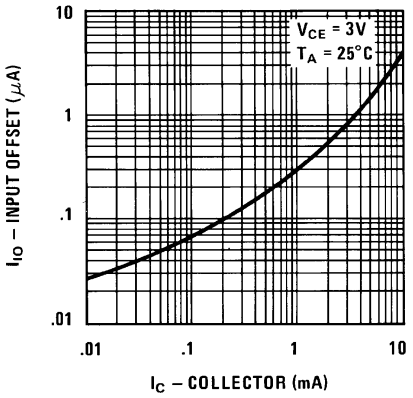

Figure 5.

Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current

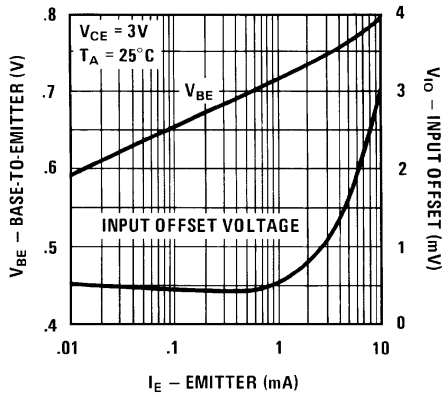

Figure 6.

Typical Base To Emitter Voltage Characteristic forEach Transistor vs Ambient Temperature

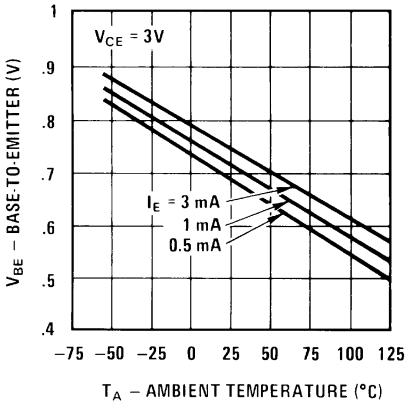

Figure 7.

Typical Performance Characteristics (continued)

Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

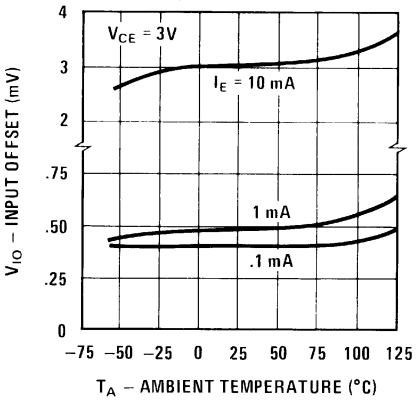

Figure 8.

Typical Noise Figure vs Collector Current

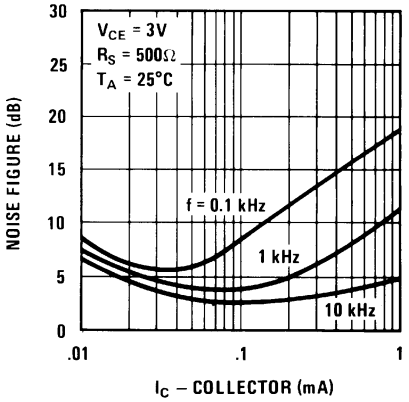

Figure 9.

Typical Noise Figure vs Collector Current

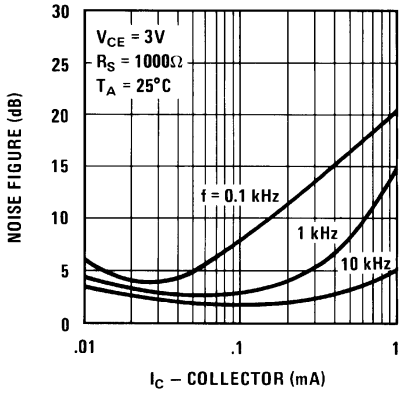

Figure 10.

Typical Noise Figure vs Collector Current

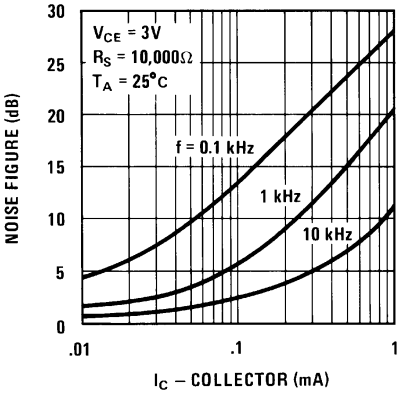

Figure 11.

Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

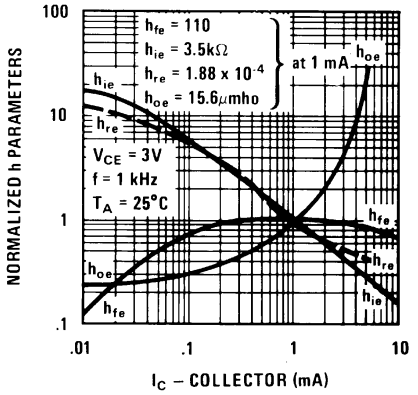

Figure 12.

Typical Forward Transfer Admittance vs Frequency

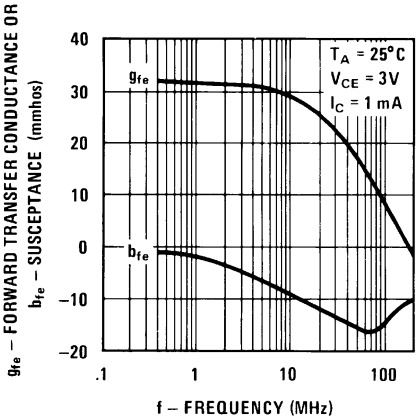

Figure 13.

Typical Performance Characteristics (continued)

Typical Input Admittance vs Frequency

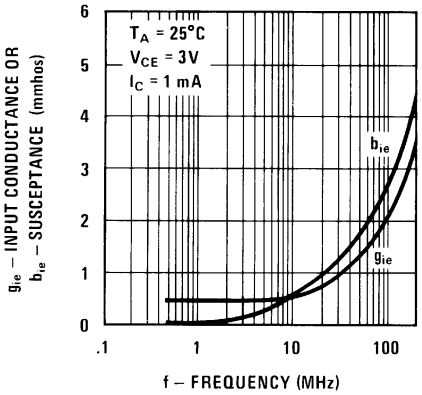

Figure 14.

Typical Output Admittance vs Frequency

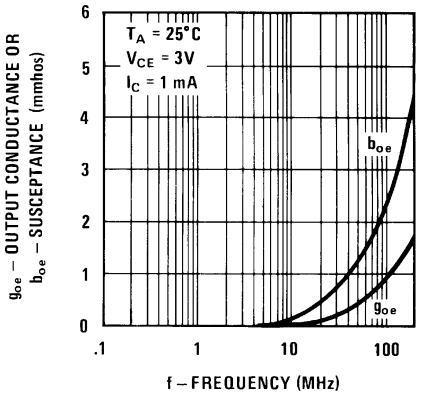

Figure 15.

Typical Reverse Transfer Admittance vs Frequency

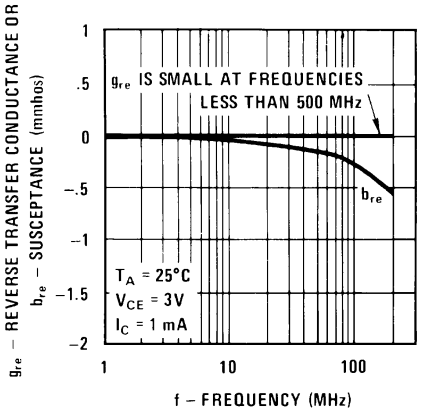

Figure 16.

Typical Gain-Bandwidth Product vs Collector Current

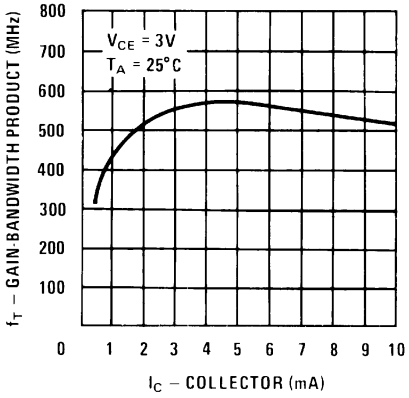

Figure 17.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3046M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM3046M	
LM3046M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM3046M	Samples
LM3046MX	NRND	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LM3046M	
LM3046MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM3046M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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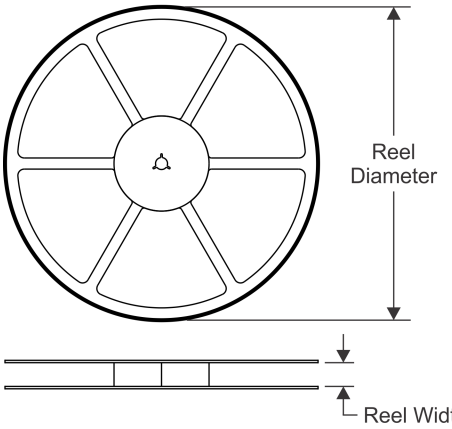
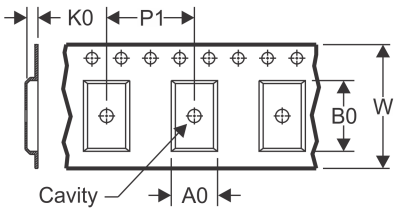
TAPE AND REEL INFORMATION

REEL DIMENSIONS

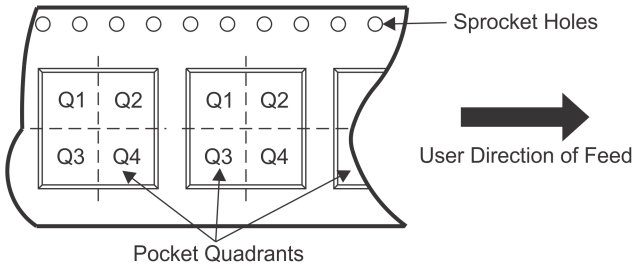


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

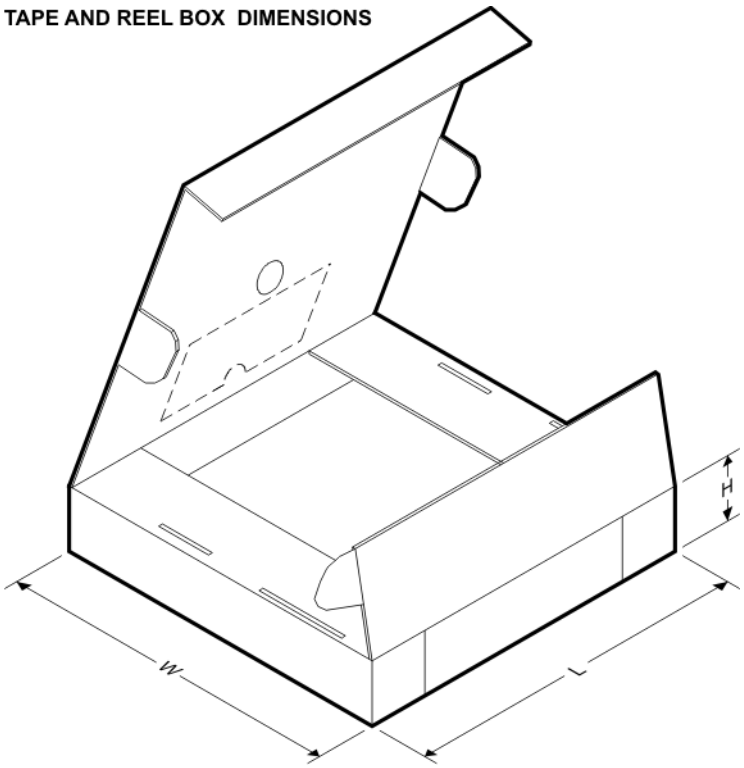
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3046MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

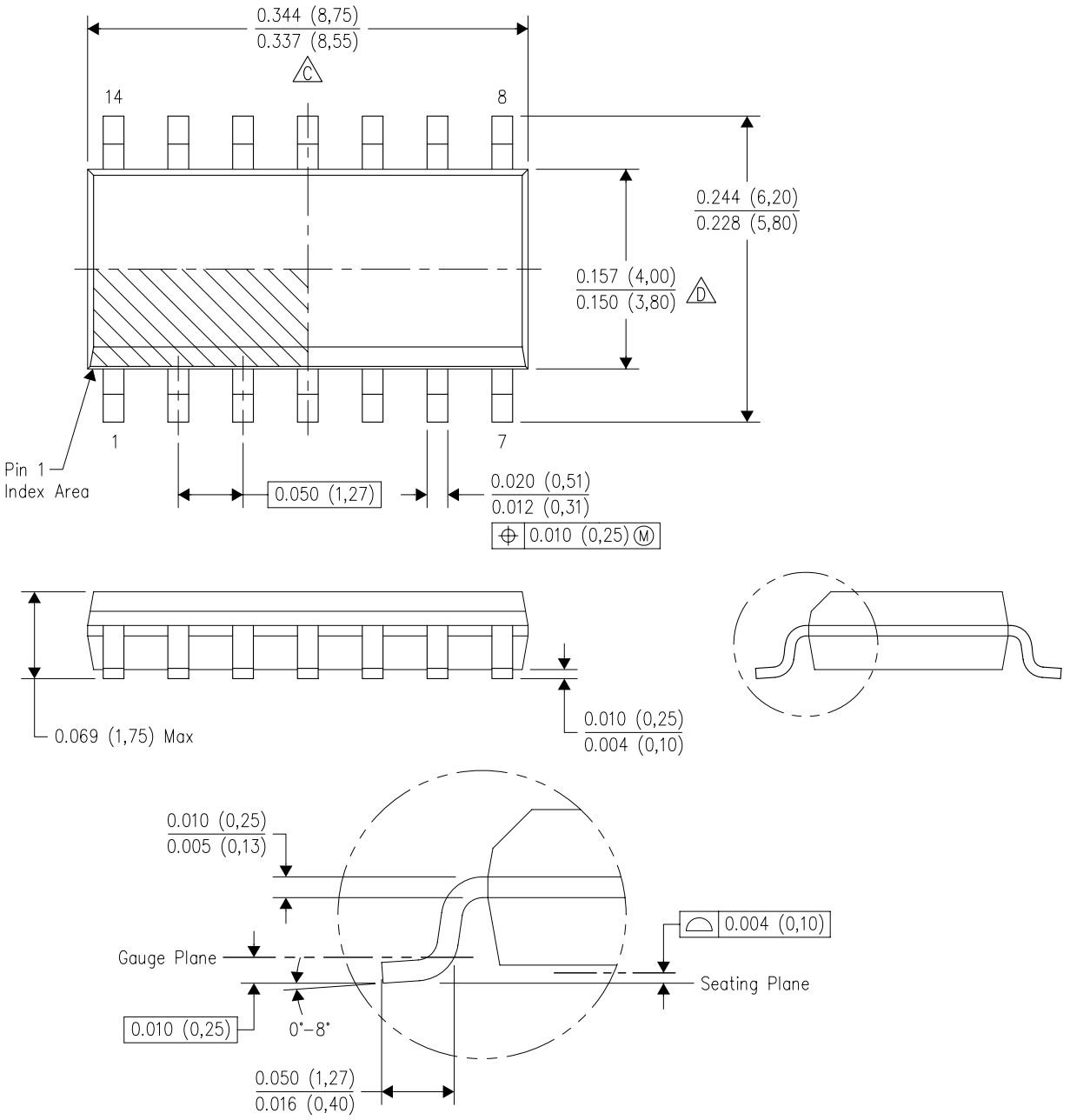
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3046MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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