



December 2015

# FSB70450 Motion SPM<sup>®</sup> 7 Series

## Features

- UL Certified No. E209204 (UL1557)
- High Performance PQFN Package
- 500 V  $R_{DS(on)} = 2.2 \Omega(\text{Max})$  FRFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving with Under-Voltage Protection and Interlock Function
- Isolation Rating: 1500 V<sub>rms</sub> / min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

## Application

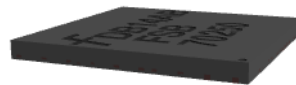
- 3-Phase Inverter Driver for Small Power AC Motor Drives

## Related Source

- [AN-9077 - Motion SPM<sup>®</sup> 7 Series User's Guide](#)
- [AN-9078 - Surface Mount Guidelines for Motion SPM<sup>®</sup> 7 Series](#)

## General Description

The FSB70450 is an advanced Motion SPM<sup>®</sup> 7 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET<sup>®</sup> technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, thermal monitoring, fault reporting and interlock function. The built-in one HVIC translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.



3D Package Drawing (Click to Activate 3D Content)

## Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSB70450	FSB70450	PQFN27A	13"	24 mm	1000 units

## Absolute Maximum Ratings

**Inverter Part** (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
$V_{DSS}$	Drain-Source Voltage of Each MOSFET		500	V
* $I_{D25}$	Each MOSFET Drain Current, Continuous	$T_{CB} = 25^{\circ}\text{C}$ (1st Notes 1)	4.8	A
* $I_{D80}$	Each MOSFET Drain Current, Continuous	$T_{CB} = 80^{\circ}\text{C}$	3.6	A
* $I_{DP}$	Each MOSFET Drain Current, Peak	$T_{CB} = 25^{\circ}\text{C}$ , $PW < 100 \mu\text{s}$	9.7	A
* $P_D$	Maximum Power Dissipation	$T_{CB} = 25^{\circ}\text{C}$ , For Each MOSFET	110	W

**Control Part** (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
$V_{DD}$	Control Supply Voltage	Applied Between $V_{DD}$ and COM	20	V
$V_{BS}$	High-side Bias Voltage	Applied Between $V_B$ and $V_S$	20	V
$V_{IN}$	Input Signal Voltage	Applied Between IN and COM	$-0.3 \sim V_{DD} + 0.3$	V
$V_{FO}$	Fault Output Supply Voltage	Applied Between FO and COM	$-0.3 \sim V_{DD} + 0.3$	V
$I_{FO}$	Fault Output Current	Sink Current FO Pin	5	mA
$V_{CSC}$	Current Sensing Input Voltage	Applied Between Csc and COM	$-0.3 \sim V_{DD} + 0.3$	V

### Total System

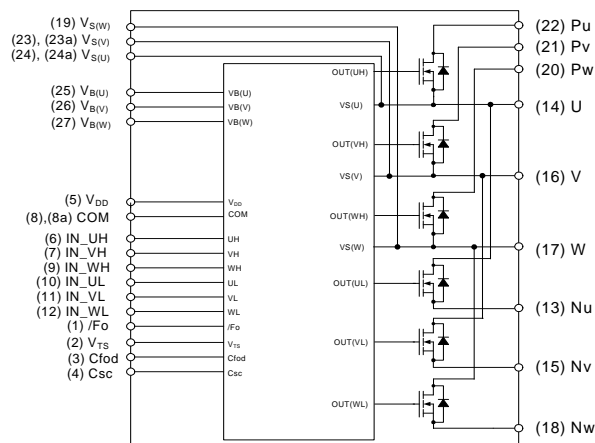
Symbol	Parameter	Conditions	Rating	Unit
$T_J$	Operating Junction Temperature		$-40 \sim 150$	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature		$-40 \sim 125$	$^{\circ}\text{C}$
$V_{ISO}$	Isolation Voltage	60 Hz, Sinusoidal, 1 Minute, Connection Pins to Heat Sink Plate	1500	$V_{rms}$

**1st Notes:**

- $T_{CB}$  is pad temperature of case bottom.
- Marking "\*" is calculation value or design factor.

## Pin descriptions

Pin Number	Pin Name	Pin Description
1	/FO	Fault Output
2	$V_{TS}$	Voltage Output of HVIC Temperature
3	Cfod	Capacitor for Duration of Fault Output
4	Csc	Capacitor (Low-pass Filter) for Short-circuit Current Detection Input
5	$V_{DD}$	Supply Bias Voltage for IC and MOSFETs Driving
6	IN_UH	Signal Input for High-side U Phase
7	IN_VH	Signal Input for High-side V Phase
8 (8a)	COM	Common Supply Ground
9	IN_WH	Signal Input for High-side W Phase
10	IN_UL	Signal Input for Low-side U Phase
11	IN_VL	Signal Input for Low-side V Phase
12	IN_WL	Signal Input for Low-side W Phase
13	Nu	Negative DC-Link Input for U Phase
14	U	Output for U Phase
15	Nv	Negative DC-Link Input for V Phase
16	V	Output for V Phase
17	W	Output for W Phase
18	Nw	Negative DC-Link Input for W Phase
19	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase MOSFETs Driving
20	$P_W$	Positive DC-Link Input for W Phase
21	$P_V$	Positive DC-Link Input for V Phase
22	$P_U$	Positive DC-Link Input for U Phase
23 (23a)	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase MOSFETs Driving
24 (24a)	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase MOSFETs Driving
25	$V_{B(U)}$	High-side Bias Voltage for U Phase MOSFETs Driving
26	$V_{B(V)}$	High-side Bias Voltage for V Phase MOSFETs Driving
27	$V_{B(W)}$	High-side Bias Voltage for W Phase MOSFETs Driving



**Figure 1. Pin Configuration and Internal Block Diagram**

**1st Notes:**

- Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM® 7 product. External connections should be made as indicated in Figure 2.
- The suffix -a pad is connected with same number pin. ex) 8 and 8a is connected inside.

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$ ,  $V_{DD} = V_{BS} = 15\text{ V}$  unless otherwise specified.)

**Inverter Part** (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$BV_{DSS}$	Drain - Source Breakdown Voltage	$V_{IN} = 0\text{ V}$ , $I_D = 1\text{ mA}$ (2nd Notes 1)	500	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{IN} = 0\text{ V}$ , $V_{DS} = 500\text{ V}$	-	-	1	mA
$R_{DS(on)}$	Static Drain - Source Turn-On Resistance	$V_{DD} = V_{BS} = 15\text{ V}$ , $V_{IN} = 5\text{ V}$ , $I_D = 1.0\text{ A}$	-	1.9	2.2	$\Omega$
$V_{SD}$	Drain - Source Diode Forward Voltage	$V_{DD} = V_{BS} = 15\text{ V}$ , $V_{IN} = 0\text{ V}$ , $I_D = -1.0\text{ A}$	-	0.9	1.2	V
$t_{ON}$	Switching Times	$V_{PN} = 300\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_D = 1.0\text{ A}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive Load $L = 3\text{ mH}$ Low-Side MOSFET Switching (2nd Notes 2)	-	600	-	ns
$t_{D(ON)}$			-	560	-	ns
$t_{OFF}$			-	660	-	ns
$t_{D(OFF)}$			-	600	-	ns
$I_{rr}$			-	1.9	-	A
$t_{rr}$			-	90	-	ns
$E_{ON}$			-	45	-	$\mu\text{J}$
$E_{OFF}$			-	8	-	$\mu\text{J}$

**Control Part** (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$I_{QDD}$	Quiescent $V_{DD}$ Current	$V_{DD}=15\text{V}$ , $V_{IN}=0\text{V}$	$V_{DD} - \text{COM}$	-	1.7	3.0	mA
$I_{QBS}$	Quiescent $V_{BS}$ Current	$V_{BS}=15\text{V}$ , $V_{IN}=0\text{V}$	$V_{B(X)}-V_{S(X)}$ , $V_{B(V)}-V_{S(V)}$ , $V_{B(W)}-V_{S(W)}$	-	45	70	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Current	$V_{DD}=15\text{V}$ , $F_{PWM}=20\text{kHz}$ , duty=50%, PWM signal input for Low side	$V_{DD} - \text{COM}$	-	1.9	3.2	mA
$I_{PBS}$	Operating $V_{BS}$ Current	$V_{BS}=15\text{V}$ , $F_{PWM}=20\text{kHz}$ , duty=50%, PWM signal input for High side	$V_{B(U)}-V_{S(U)}$ , $V_{B(V)}-V_{S(V)}$ , $V_{B(W)}-V_{S(W)}$	-	300	400	$\mu\text{A}$
$UV_{DDD}$	Low-side Undervoltage Protection (Figure 6)	$V_{DD}$ Undervoltage Protection Detection Level	7.4	8.0	9.4	V	
$UV_{DDR}$		$V_{DD}$ Undervoltage Protection Reset Level	8.0	8.9	9.8	V	
$UV_{BSD}$	High-side Undervoltage Protection (Figure 7)	$V_{BS}$ Undervoltage Protection Detection Level	7.4	8.0	9.4	V	
$UV_{BSR}$		$V_{BS}$ Undervoltage Protection Reset Level	8.0	8.9	9.8	V	
$V_{TS}$	HVIC Temperature sensing voltage output	$V_{DD}=15\text{V}$ , $T_{HVIC}=25^\circ\text{C}$ (2nd Notes 3)	580	675	770	mV	
$V_{IH}$	ON Threshold Voltage	Logic High Level	IN - COM	-	-	2.4	V
$V_{IL}$	OFF Threshold Voltage	Logic Low Level		0.8	-	-	V
$V_{SC(ref)}$	SC Current Trip Level	$V_{DD}=15\text{V}$	$C_{SC} - \text{COM}$	0.45	0.5	0.55	V
$t_{FOD}$	Fault-out Pulse Width	$C_{FOD}=33\text{nF}$ (2nd Note 4)	1.0	1.4	1.8	ms	

**2nd Notes:**

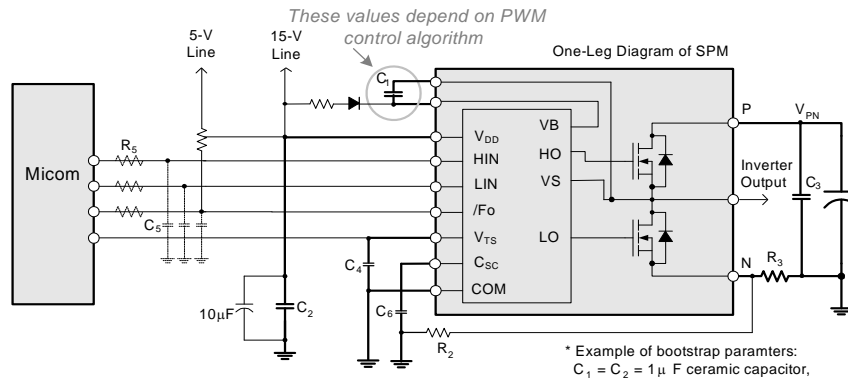
- $BV_{DSS}$  is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM® 7 product.  $V_{PN}$  should be sufficiently less than this value considering the effect of the stray inductance so that  $V_{PN}$  should not exceed  $BV_{DSS}$  in any case.
- $t_{ON}$  and  $t_{OFF}$  include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 3 for the switching time definition with the switching test circuit of Figure 4.
- $V_{TS}$  is only for sensing-temperature of module and cannot shutdown MOSFETs automatically.
- The fault-out pulse width  $t_{FOD}$  depends on the capacitance value of  $C_{FOD}$  according to the following approximate equation :  $C_{FOD} = 24 \times 10^{-6} \times t_{FOD} [F]$

## Recommended Operating Condition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply Voltage	Applied Between P and N	-	300	400	V
$V_{DD}$	Control Supply Voltage	Applied Between $V_{DD}$ and COM	13.5	15.0	16.5	V
$V_{BS}$	High-Side Bias Voltage	Applied Between $V_B$ and $V_S$	13.5	15.0	16.5	V
$dV_{DD}/dt$ , $dV_{BS}/dt$	Control Supply Variation		-1.0	-	1.0	V/ $\mu$ s
$t_{dead}$	Blanking Time for Preventing Arm-Short	$V_{DD} = V_{BS} = 13.5 \sim 16.5$ V, $T_J \leq 150^\circ\text{C}$	500	-	-	ns
$f_{PWM}$	PWM Switching Frequency	$T_J \leq 150^\circ\text{C}$	-	15	-	kHz

## Thermal Resistance

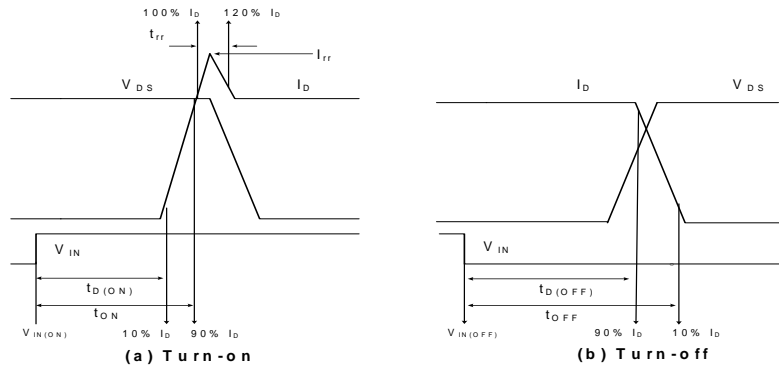
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JCB}$	Junction to Case Bottom Thermal Resistance	Single MOSFET Operating Condition (3rd Notes 1)	-	0.9	-	$^\circ\text{C}/\text{W}$



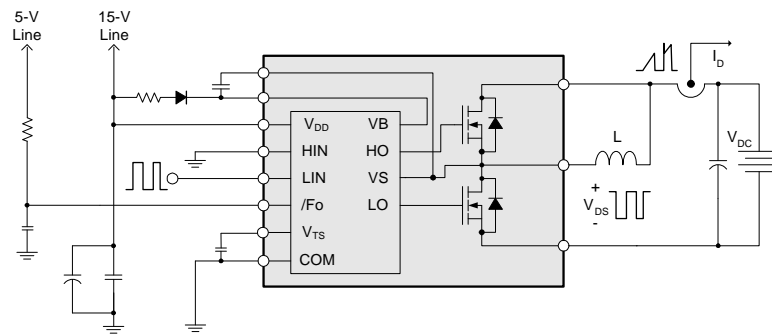
**Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters**

### 3rd Notes:

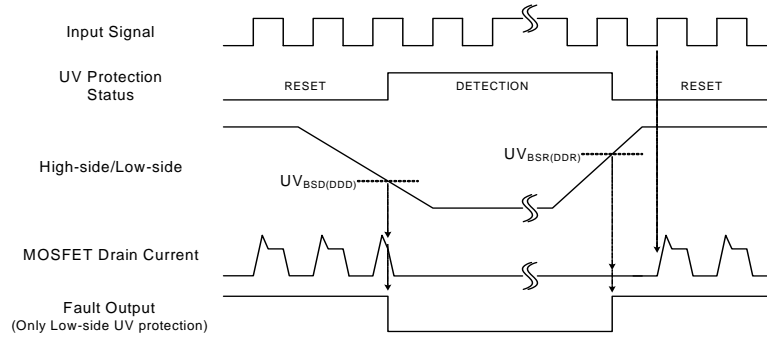
- $R_{\theta JCB}$  is simulation value with application board layout. (Please refer user's guide SPM7 series)
- Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- RC coupling ( $R_5$  and  $C_5$ ) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outputs.
- Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage.



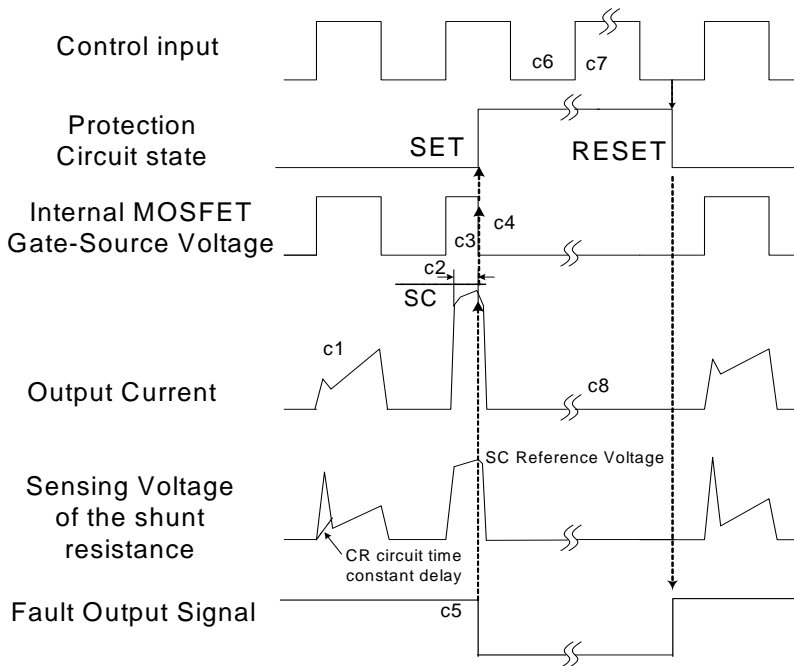
**Figure 3. Switching Time Definition**



**Figure 4. Switching Test Circuit (Low-side)**



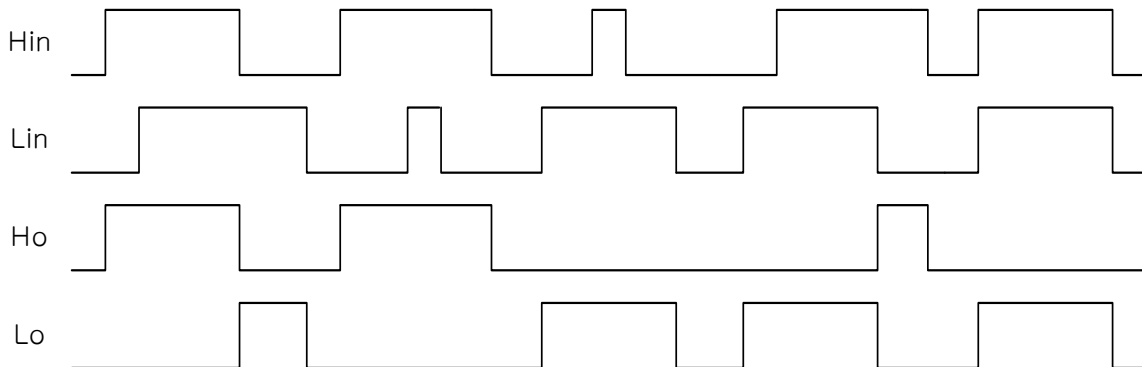
**Figure 5. Under Voltage Protection**



**Figure 6. Short-Circuit Current Protection**

(with the external shunt resistance and CR connection)

- c1 : Normal operation: MOSFET ON and carrying current.
- c2 : Short circuit current detection (SC trigger).
- c3 : Hard MOSFET gate interrupt.
- c4 : MOSFET turns OFF.
- c5 : Fault output timer operation start : Fault-out width ( $t_{FOD}$ )
- c6 : Input "L" : MOSFET OFF state.
- c7 : Input "H" : MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.
- c8 : MOSFET OFF state



**Figure 7. Timing Chart of Interlock Function**

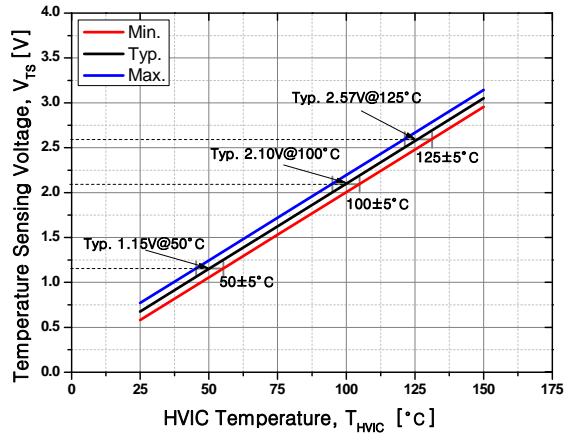


Figure 8. Temperature profile  $V_{TS}$  vs.  $T_{HVIC}$

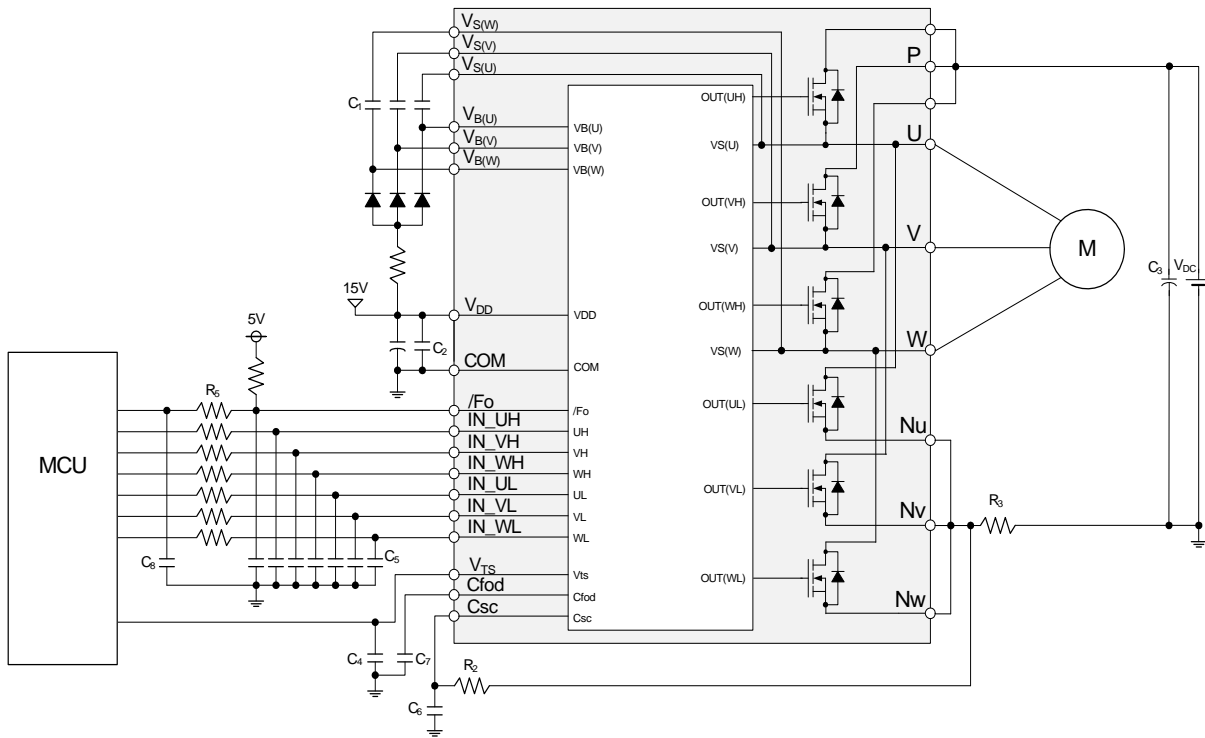
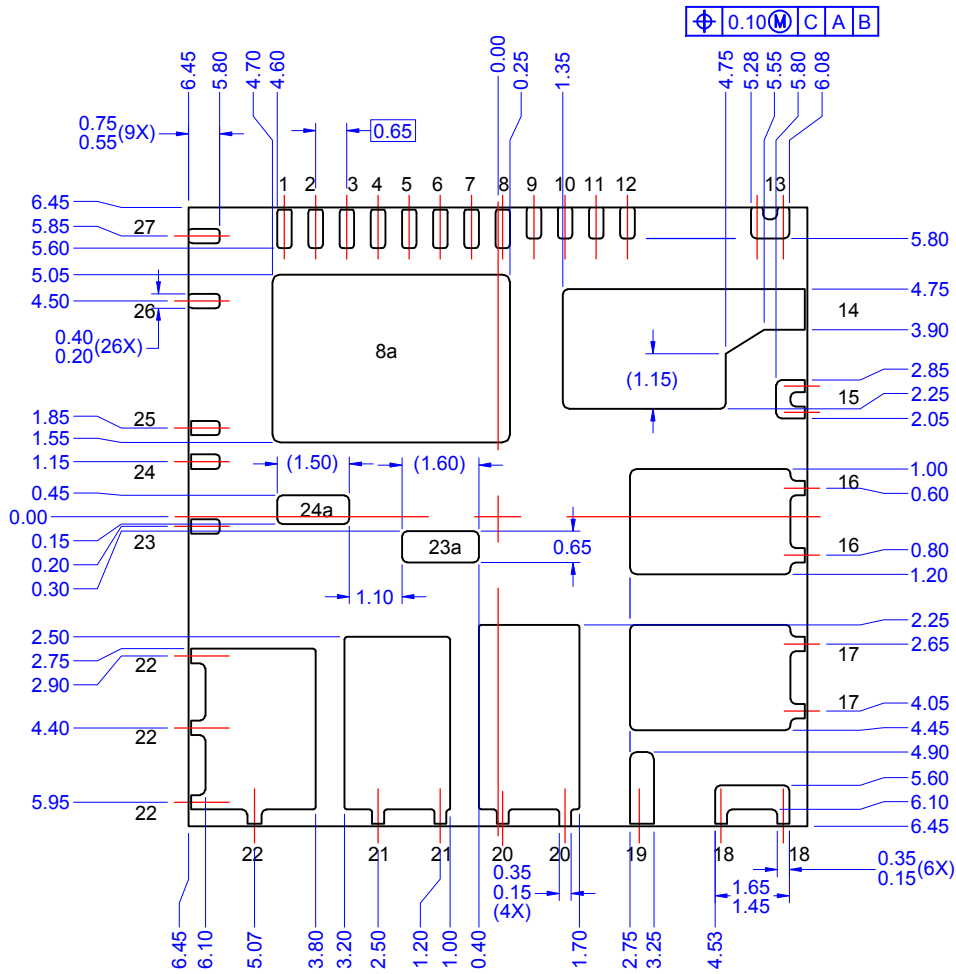


Figure 9. Example of Application Circuit

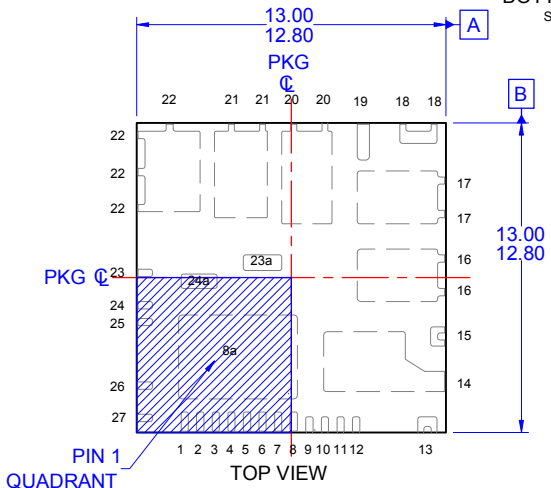
**4th Notes:**

1. RC-coupling ( $R_5$  and  $C_5$ ,  $R_2$  and  $C_6$ ) and  $C_1$ ,  $C_5$ ,  $C_7$ ,  $C_8$  at each input of Motion SPM® 7 product and MCU are useful to prevent improper input signal caused by surge-noise.
2. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
3. All the filter capacitors should be connected close to Motion SPM 7 product, and they should have good characteristics for rejecting high-frequency ripple current.

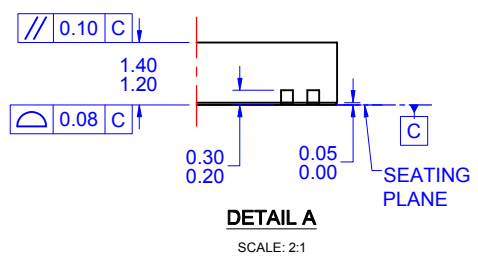




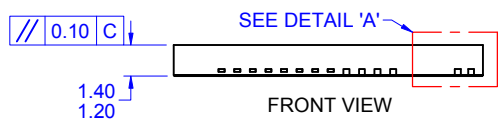
BOTTOM VIEW  
SCALE: 2:1



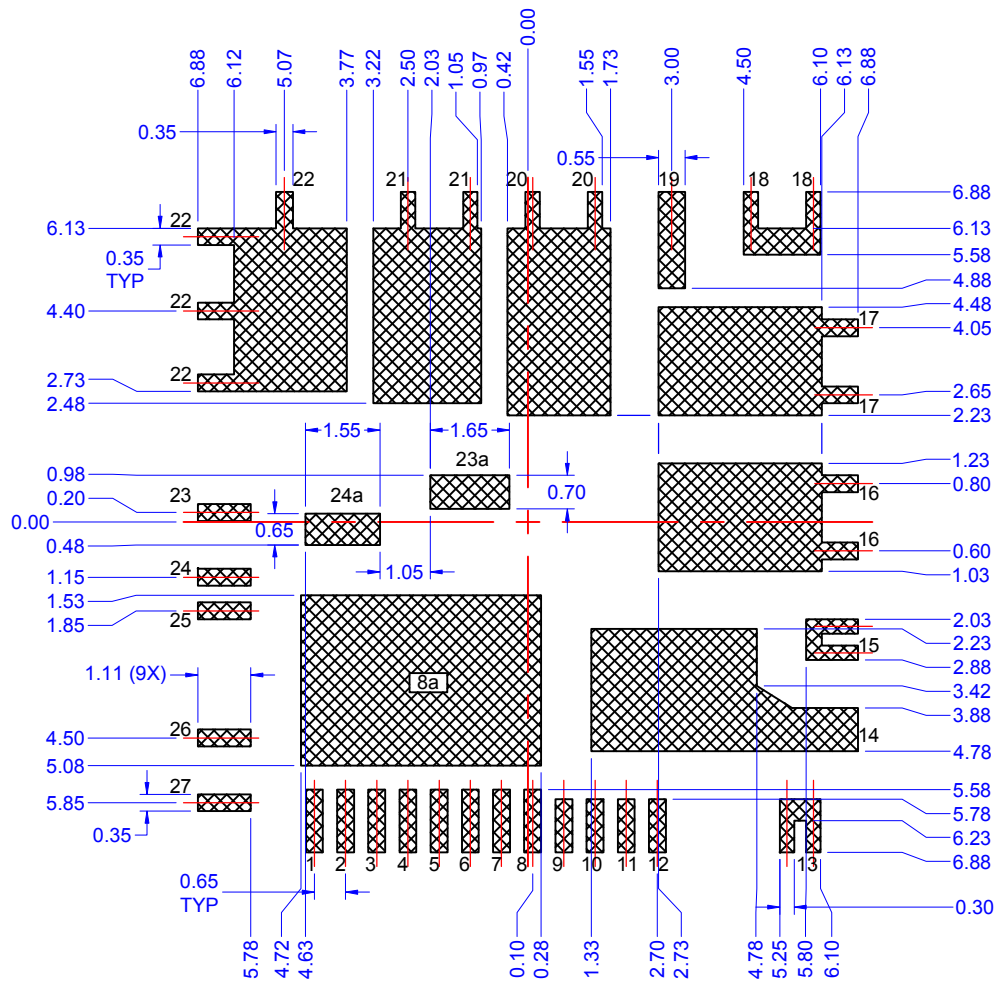
TOP VIEW



DETAIL A  
SCALE: 2:1



FRONT VIEW



LAND PATTERN  
RECOMMENDATION  
SCALE: 2:1

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- D) DRAWING CONFORMS TO ASME Y14.5M-1994.
- E) LAND PATTERN REFERENCE:  
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- F) DRAWING FILE NAME: MKT-PQFN27AREV3.
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