Enpirion® Power Datasheet

EC2630QI 4.5A, 27W 12V DC-DC Intermediate Voltage Bus Converter

Description

The EC2630QI is a high density, high efficiency DC-DC intermediate voltage bus converter which generates an output voltage that tracks one half the input voltages and is designed to provide power to Altera's highly integrated Enpirion DC-DC point-of-load converter products for a complete 12V solution. EC2630QI provides the means to condition power from a 12V input, to supply multiple lower voltage converters while enabling high efficiency and small PCB area. Due to its extremely high efficiency, it avoids the common two stage power conversion penalty and is equivalent to or better than direct regulation.

This Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings. All of Altera's Enpirion products are RoHS compliant.

Features

- Complete power conditioning solution from a 12 volt power bus.
- 5.5mm x 5.5mm x 3mm QFN Package.
- Total solution size of 228mm^2.
- Input voltage range of 10V to 13.2V.
- The output voltage is half the input voltage.
- High and flat efficiency, up to 97.5%.
- 4.5A Continuous Output Current Capability.
- Adjustable operating frequency with optional external clock input.
- Master/Slave Mode for Parallel Operation.
- Output VIN_OK pin.
- Thermal shutdown, short circuit, Overcurrent, and UVLO protection.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Applications requiring down conversion from a 12V bus to an output voltage with high efficiency.
- Systems requiring multiple voltage rails such as FPGA and ASIC.
- Enterprise, Industrial, Embedded, and Telecommunication applications.
- Multi-rail computer & network interface applications such as PCIe and ATCA AMC cards.
- 12V Industrial and Consumer Applications such
- as Audio/Video Home Theater, Tuners

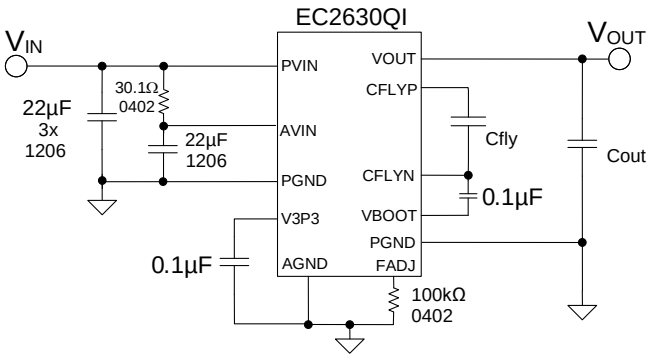


Figure 1. Typical Application Schematic Optimized for Maximum Efficiency

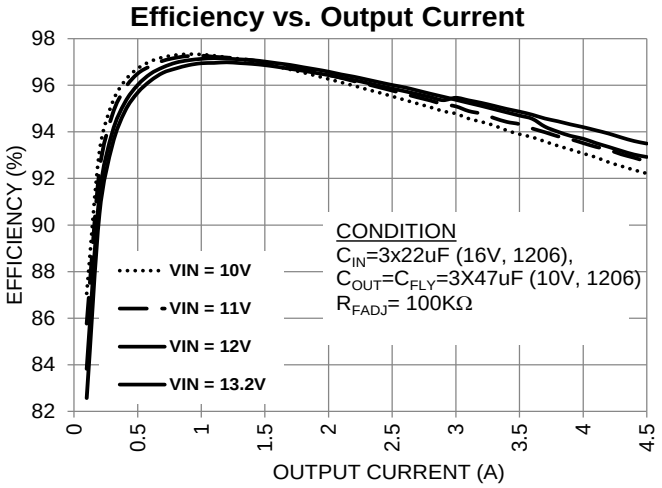


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
EC2630QI	EC2630QI	-40 to +85	36 pin (5.5mm x 5.5mm x 3mm) QFN Package
EVB-EC2630QI	EC2630QI	QFN Evaluation Board	

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

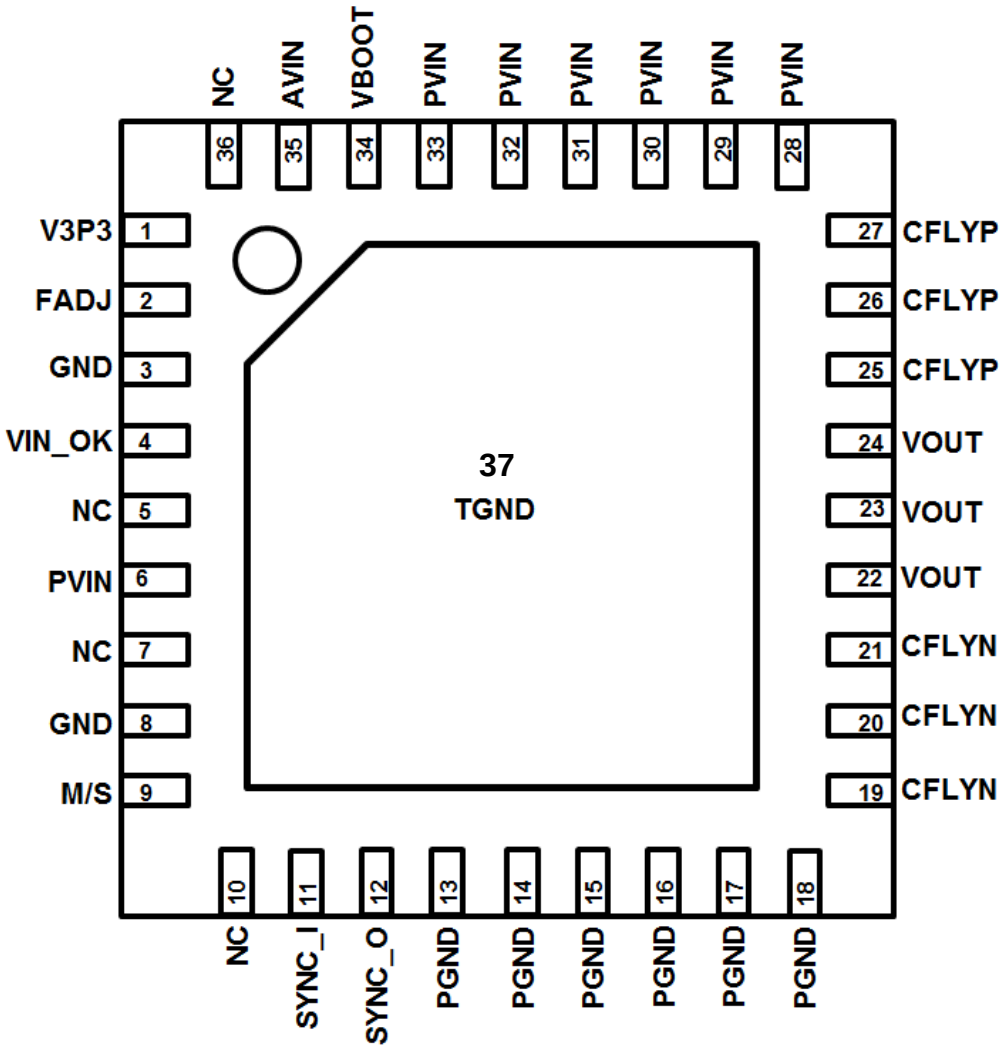


Figure 3. Pin-out diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
NOTE B: The white dot on the top left of the device package is the pin-1 indicator.

Pin Descriptions

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/output

PIN	NAME	I/O	FUNCTION
1	V3P3	O	Internal Regulated Supply Output. Connect bypass capacitor from V3P3 to GND.
2	FADJ	I/O	Frequency Adjust pin used to set the switching frequency. See Theory of Operation Section for selecting the required resistor.
3, 8	GND	G	Internally Regulated Supply Ground. Must tie directly to ground plane with a via right next to each pin.
4	VIN_OK	O	Open drain transistor for power system state indication for nominal 12V operation. VIN_OK is logic high when Vin is greater than 9V. This pin can be used to control the ENABLE signals of downstream converters powered by the EC2630.
5, 7, 10, 36	NC	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION: May be internally connected.
6	PVIN	P	Main Input Supply
9	M/S	I	Master/Slave pin for clock synchronization. Logic low = Master. Logic high = Slave. Use in master mode for standalone devices.
11	SYNC_I	I	External Synchronizing Clock Input, input accepted in Slave mode from an EC2630 operating in master mode. May be left floating when used in master mode.
12	SYNC_O	O	Synchronizing Clock Output. Provides clock input to EC2630s in slave mode.
13-18	PGND	G	Power ground for the switching voltage attenuator
19-21	CFLYN	I/O	Negative Terminal of Flying Capacitor
22-24	VOUT	O	Converter Output Voltage
25-27	CFLYP	I/O	Positive Terminal of Flying Capacitor
28-33	PVIN	P	Main Input Supply
34	VBOOT	I/O	Internal power Supply for high-side drive. Connect a 0.1uF/25V boot-strap capacitor from VBOOT to CFLYN.
35	AVIN	P	Quiet Input Supply for Controller. Connect to PVIN through an RC filter. Refer to application schematics for details
37	TGND	G	This pad is a thermal ground. It must be thermally and electrically connected to the ground plane through a matrix of vias.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage – PVIN, AVIN	V_{IN}	-0.5	13.5	V
Input Voltage – VIN_OK, CFLYN, CFLYP, Vout		-0.5	VIN	V
Input Voltage – V3P3, FADJ, M_S, SYNC_I, SYNC_O		-0.5	3.5	V
Input Voltage – VBOOT		-0.5	VIN + 8	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ MAX}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model): AVIN	Positive Negative	1500 2000		V
ESD Rating (based on Human Body Model): All other pins		2000		V
ESD Rating (based on Charged Device Model)		500		V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	10	12	13.2	V
Continuous Output Current	I_{OUT_MAX}			4.5	A
Operating Junction Temperature	T_J	-40		+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Thermal Shutdown	T_{SD}		155		°C
Thermal Shutdown Hysteresis	T_{SDH}		25		°C
Thermal Resistance: Junction to Case	θ_{JC}		1		°C/W
Thermal Resistance: Junction to Ambient	θ_{JA}		19		°C/W

Electrical Characteristics

NOTE: V_{IN}=12.0V over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

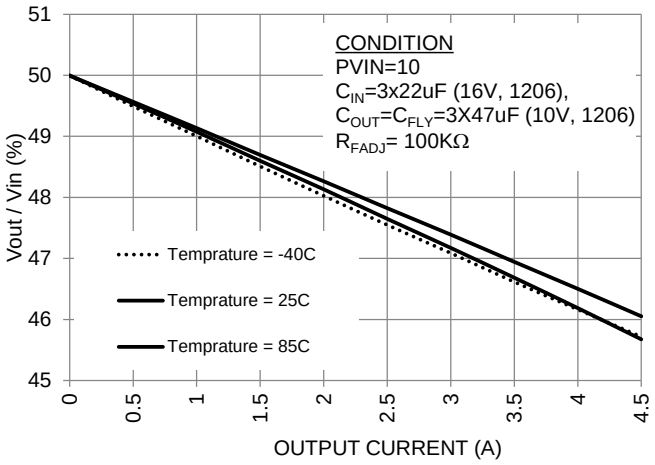
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Boot Strap Voltage	VBOOT	@ Vin =12V, with 0.1uF capacitor between VBOOT and CFLYN		17		V
Internal Regulated Supply Output	V3P3	@ Vin =12V	2.97	3.3	3.63	V
Input under Voltage Lockout	V_{UVLO}		4.5	5	5.5	V
Input Voltage Indication Rising	VIN_OK		8	9	10	V
Input Voltage Indication Falling	VIN_OK		7	8	9	V
No-Load Operating Current	I_{OP}	@ 12V input and 125kHz switching		16		mA
Switching Frequency (Internal Oscillator)	F_{OSC}	R_{FADJ}= 100 KΩ,	68	115	165	kHz
Frequency Adjust Voltage	V_{FADJ}			1.2		V
Output Voltage as a fraction of input voltage [1]	V_{OUT}	10V ≤ V_{IN} ≤ 13.2V, 0A ≤ I_{LOAD} ≤ 4A	45		50	%
Output Impedance	R_{OUT}	$\Delta V_{OUT}/\Delta I_{LOAD}$ R_{FADJ}= 100 KΩ,		90		mΩ
Overcurrent Trip Level	V_{OCP}	Vin=12V. Overcurrent sensed as a drop in output voltage		5.2		V
M_S input Logic Low	M_S_I_VIL		-0.3		0.3	V
M_S input Logic High	M_S_I_VIH		V3P3-0.6	V3P3	V3P3 + 0.3	V
Clock Input Logic Low	SYNC_I_VIL				0.3	V
Clock Input Logic High	SYNC_I_VIH		1.8		3.3	V
Clock Output Logic Low	SYNC_O_VOL				0.3	V
Clock Output Logic High	SYNC_O_VOH	@ 1mA	V3P3-0.6			V

[1] Altera recommends that Cfly=Cout.

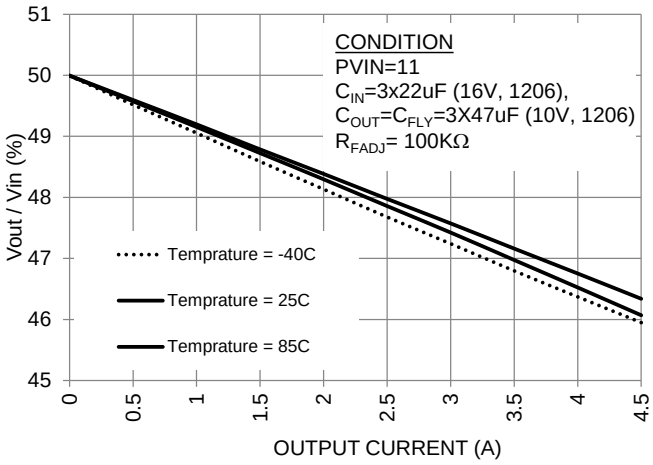
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN_OK, sink capability				1		mA
Current Balance	ΔI_{OUT}	With 2 to 4 Converters in Parallel, the Difference Between Nominal and Actual Current Levels.		+/-10		%

Typical Performance Curves

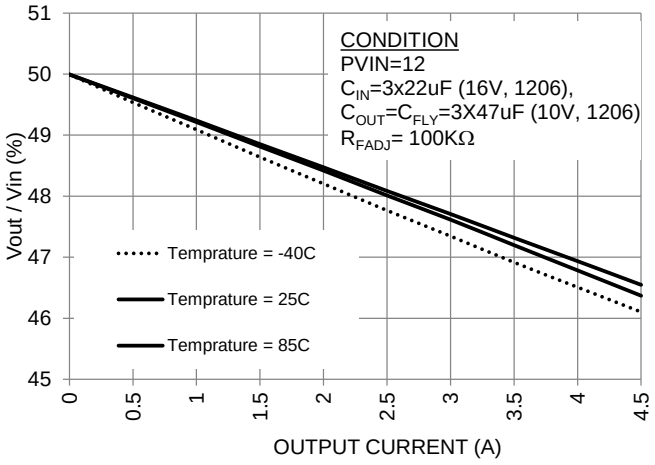
Output Voltage as a fraction of VIN at different Temperature



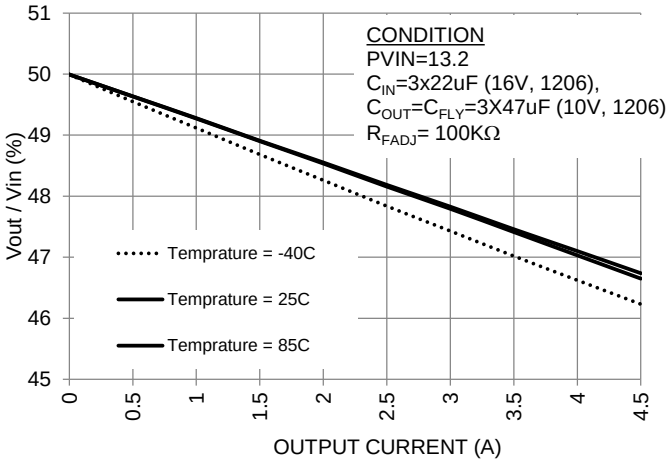
Output Voltage as a fraction of VIN at different Temperature



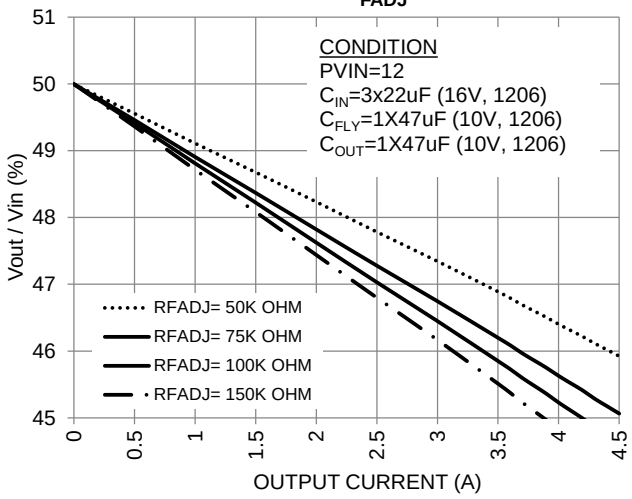
Output Voltage as a fraction of VIN at different Temperature



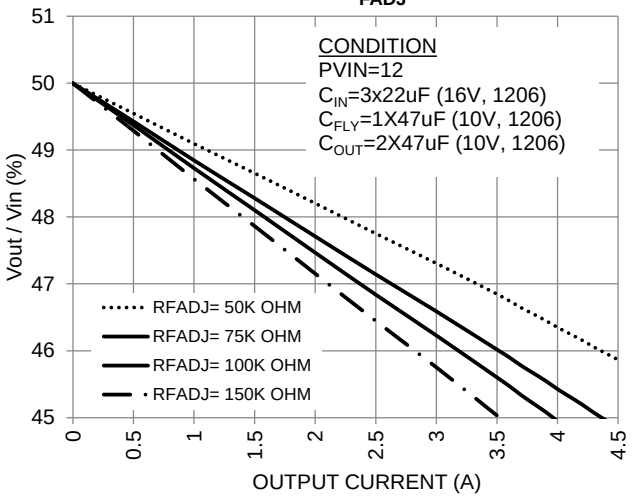
Output Voltage as a fraction of VIN at different Temperature



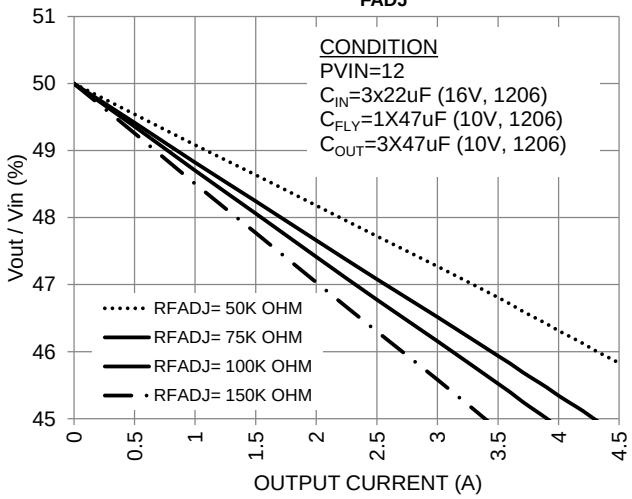
Output Voltage as a fraction of VIN at different R_{FADJ}



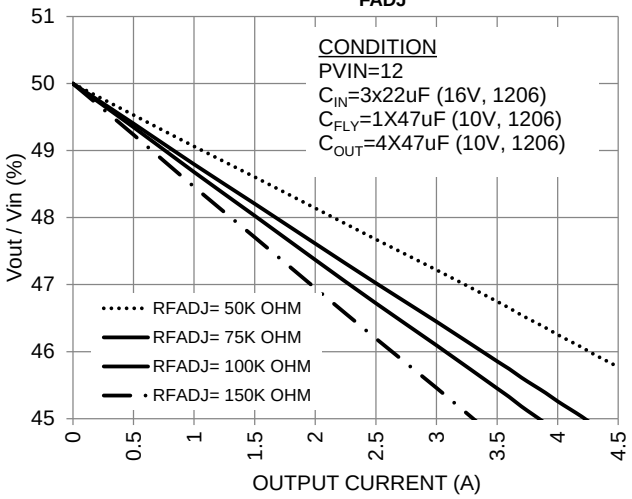
Output Voltage as a fraction of VIN at different R_{FADJ}



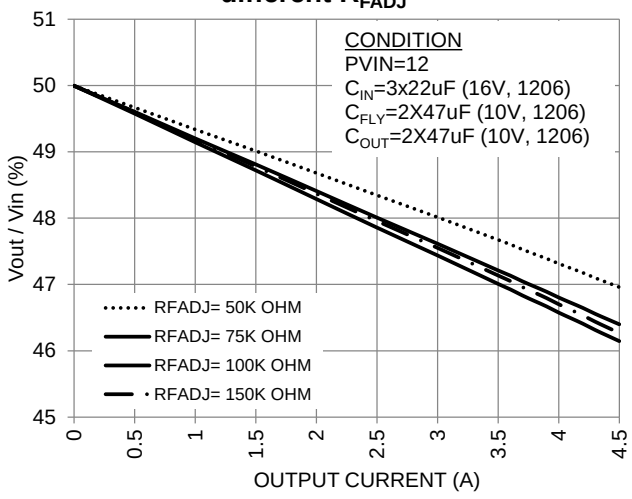
Output Voltage as a fraction of VIN at different R_{FADJ}



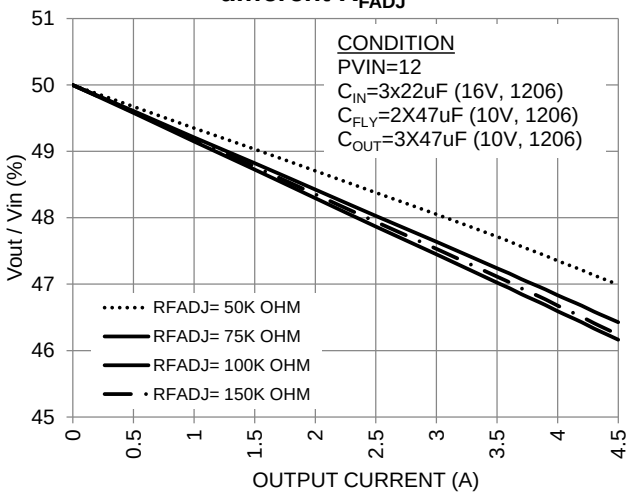
Output Voltage as a fraction of VIN at different R_{FADJ}



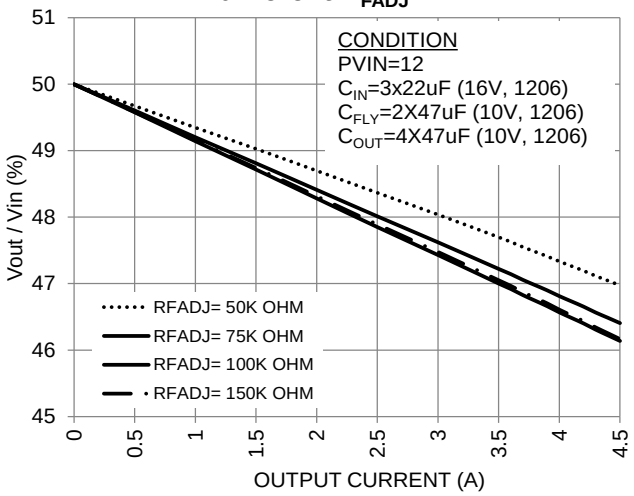
Output Voltage as a fraction of VIN at different R_{FADJ}



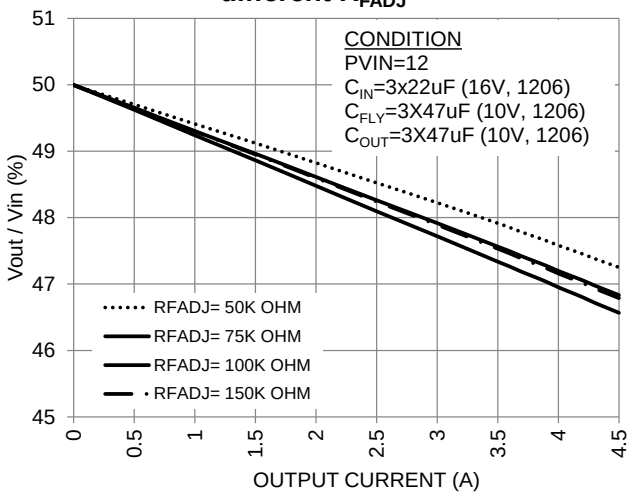
Output Voltage as a fraction of VIN at different R_{FADJ}



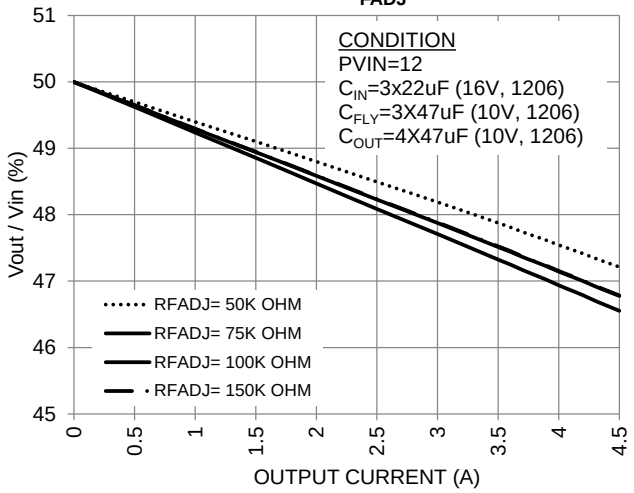
Output Voltage as a fraction of VIN at different R_{FADJ}



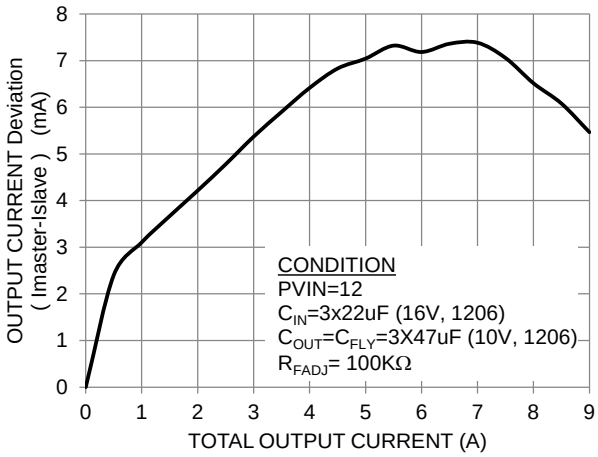
Output Voltage as a fraction of VIN at different R_{FADJ}



Output Voltage as a fraction of VIN at different R_{FADJ}

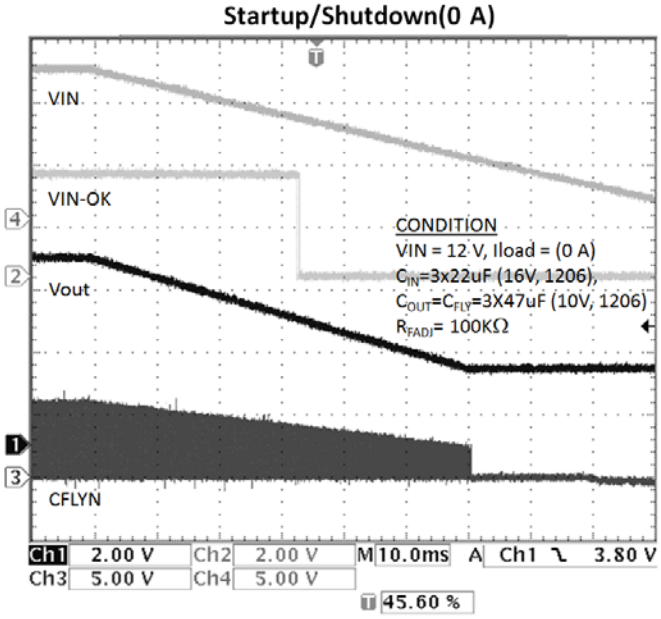


Parallel current Deviation

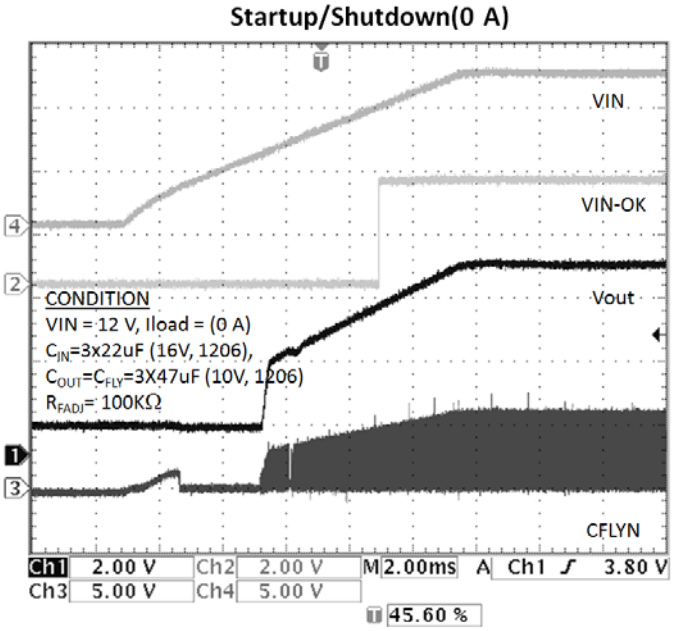


Typical Performance Characteristics

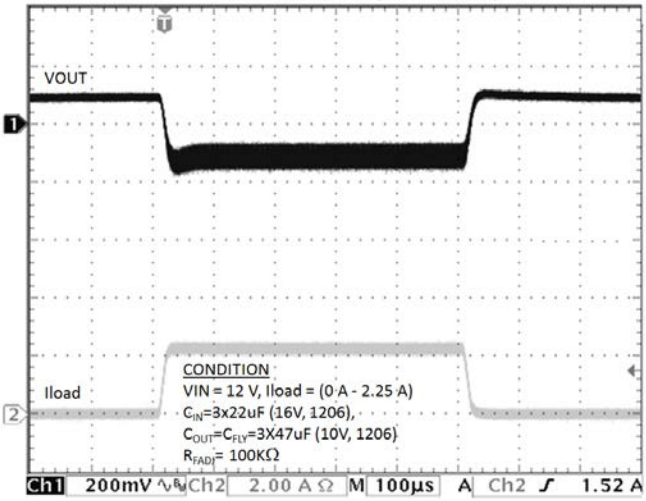
Startup/Shutdown(0 A)



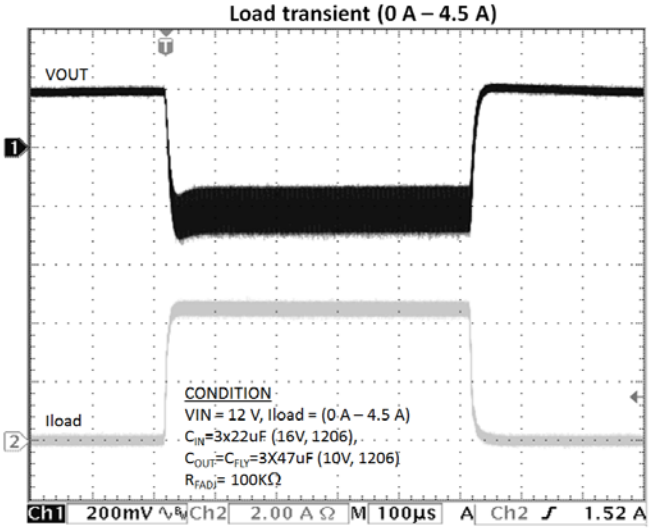
Startup/Shutdown(0 A)



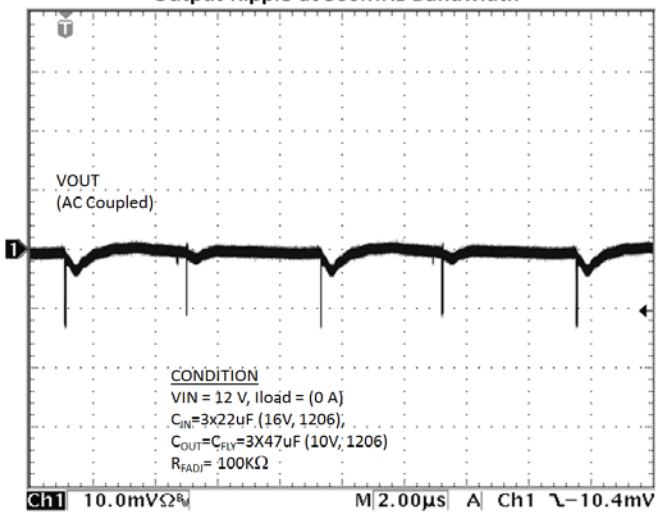
Load transient (0 A - 2.25 A)



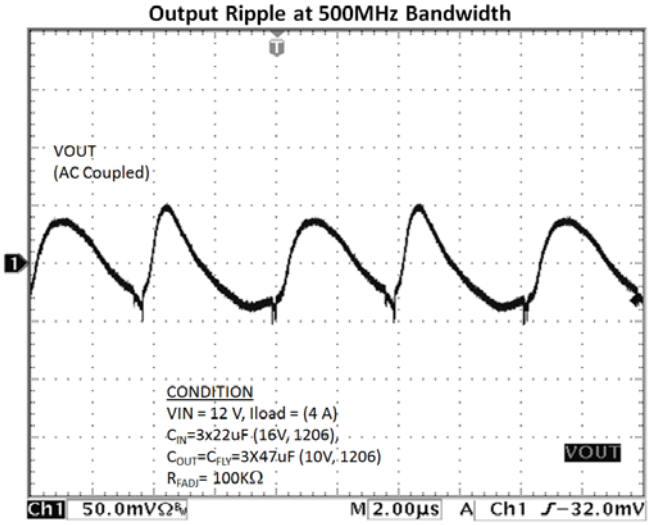
Load transient (0 A – 4.5 A)



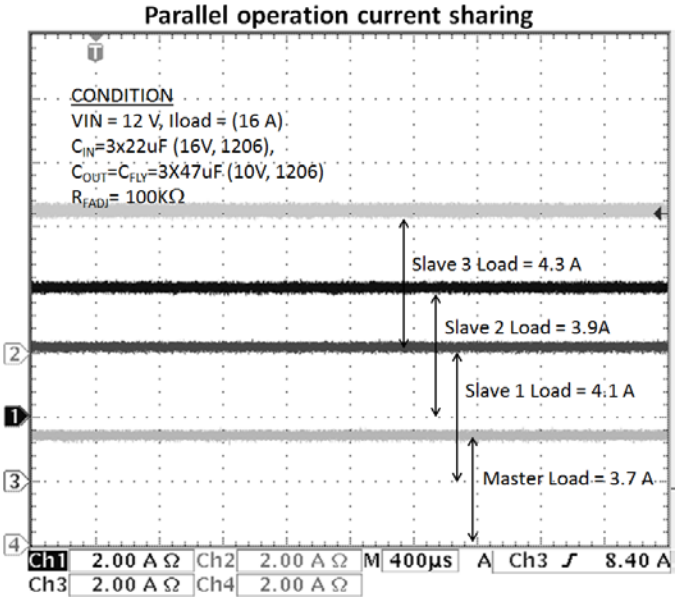
Output Ripple at 500MHz Bandwidth



Output Ripple at 500MHz Bandwidth



Parallel operation current sharing



Functional Block Diagram

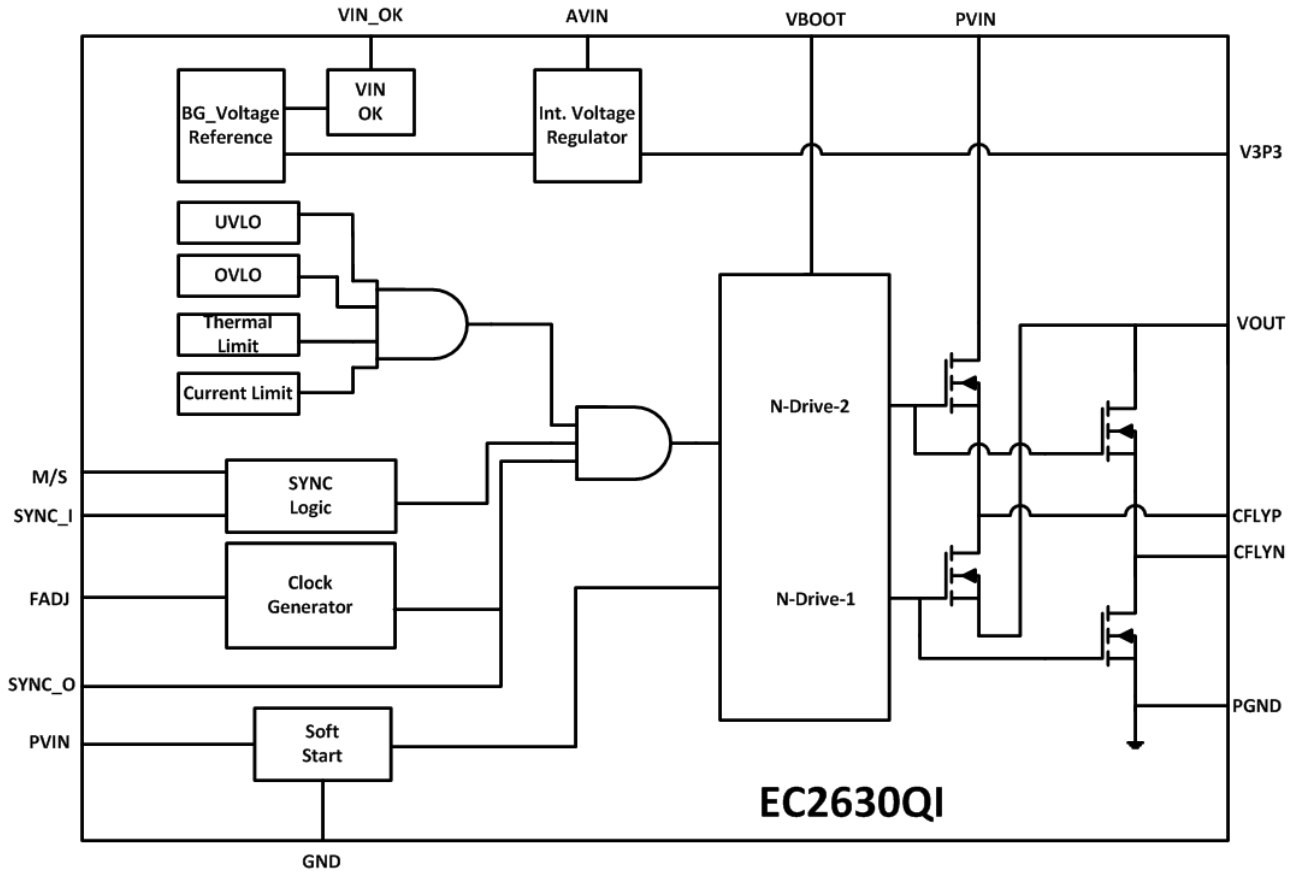


Figure 4. Functional Block Diagram

Theory of Operation

Bus Voltage Divider

The EC2630QI is an open loop voltage divider. It generates an output voltage which is approximately half the input voltage value. The device uses switched capacitors to divide the input voltage by a factor of 2. External capacitors are charged in series during one half of a clock cycle and the capacitors are then connected in parallel during the second half of the clock cycle. The output voltage depends on the input voltage and the load current.

This device has been designed specifically for use with Altera's Enpirion point-of-load products for output voltage regulation.

The Voltage Divider has the following features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 5V.
- Switching frequency is internally generated. However, a clock signal from a Master EC2630QI may be applied externally when the device is configured in Slave mode.
- When in Master mode, the device will output its internal clock to the SYNC_O pin.
- Soft-start circuit, to limit the in-rush current when the converter is powered up.
- VIN_OK indicator signal.

Frequency Synch (Master/Slave)

In Master mode, the internal switching frequency of the Master device is output through SYNC_O pin. This clock signal can be used to drive other EC2630QI devices for synchronization or parallel operation. In Slave mode, a master device's SYNC_O pin provides the clock input by connecting it to the slave device's SNYC_I pin. Note that in order for the device to function properly in slave mode, it has to be clocked from a valid EC2630QI master device. Applying an external signal/clock to the SYNC_I pin might cause unpredicted operation and potentially damage the device.

Soft-Start Operation

Soft start is a means to reduce the in-rush current when the device is enabled.

When the device is enabled by ramping up the input voltage, and the output capacitors are discharged, a large current flow is averted by modulating the gate drive of the NFET during the soft start interval. This interval is pre-programmed and not user programmable.

Overcurrent Protection

The overcurrent function is achieved by sensing the output voltage. An overcurrent state is entered when the device is out of soft start and the output voltage drops below ~85% of the expected voltage. This overcurrent state will initiate a fresh soft-start and the device will continue cycling through soft-start as long as the overcurrent condition exists.

Note that the over current protection level is dependent on the switching frequency and the output capacitance. From the below table, we can achieve a lower over current protection level by decreasing the switching frequency or the output capacitance.

	OCP Level			
R_{FADJ} / Cout=Cfly	**100K**	**150K**	**200K**	**250K**
1x47 uF	5.5	4.3	2.9	2.9
2x47 uF	8.4	7	4.7	4.8
3x47 uF	9	8.6	6.6	5.9
4x47 uF	10.5	9.5	7.5	6.7

- Altera has observed that current conditions over 6A while VOUT is regulating at VIN/2 can lead to device failure.

Thermal Overload Protection

Thermal shutdown will disable operation when the Junction temperature exceeds the value given in the Thermal Characteristics table. Once the junction temperature drops by the hysteresis temperature, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage of ~5V. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Frequency Adjustment

The device is optimized to run at 125 kHz switching frequency (with R_{FADJ}= 100 kΩ) independent of load current. The internal oscillator frequency can be adjusted by altering the value of the resistor between the FADJ pin and AGND (see chart below).

Recomended R_{FADJ} vs. SW Frequency

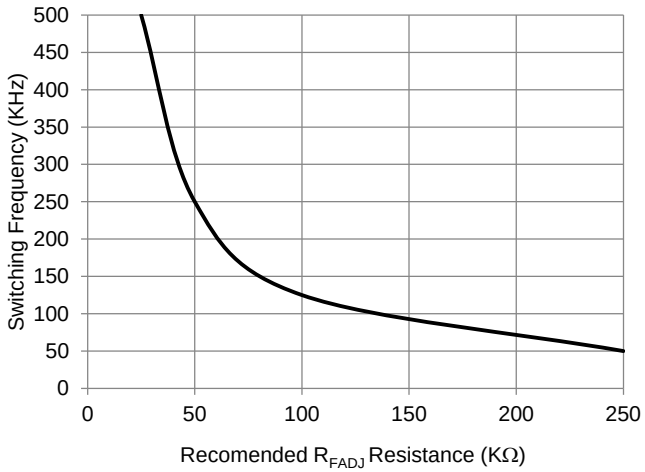


Figure 5. Recommended R_{FADJ} vs. switching frequency

Capacitor Selection

The EC2630QI requires a range of capacitance depending on application configuration. Capacitor selection is dependent upon power level, efficiency, space, and cost requirements. Low-cost, low-ESR X5R or X7R ceramic capacitors should be used. Either 1206 or 1210 case sizes are recommended. In general, 1210 capacitors exhibit less voltage coefficient than 1206 capacitors, providing more capacitance per unit volume-volt. Y5V or equivalent dielectric formulations must not be used as they lose capacitance with frequency, temperature and bias voltage.

Output capacitor and fly capacitor consideration:

Altera recommends that the Cfly value is roughly matched to the value of Cout. Note that except where indicated otherwise, the guaranteed values

and charts provided in the datasheet, including the ones for load regulation, hold good only under this condition (Cout=Cfly). For applications where there is a large mismatch between Cfly and Cout, the curves relating output voltage to Cout/Cfly ratio over load and frequency (provided in the Typical Performance Curves section) may be used to predict device operation.

Capacitor selection guidelines to support full output load (4.5A):

- Input Capacitors-
  A typical implementation might use 3x22µF, 16V 1206, MLCC capacitors
- Output Capacitors-
  As EC2630 is used to power up downstream Altera Enpirion point-of-load (POL) converters, the input capacitors for the downstream POL converters are the output capacitors for the EC2630QI. It only requires an additional local output capacitor (1x10µF). Wherever possible, it is recommended to have the downstream converters close to the bus converter.
  - The minimum implementation for output capacitor (10µF local cap + the input caps for the downstream POL) might use (1X47µF + 1x10µF), 10V, and 1206 output.
  - The maximum implementation might use (4X47µF), 10V, and 1206 output.

- Flying Capacitors-
  Flying capacitors are approximately equal to the output capacitors, and a typical implementation might use 3x47µF, 10V, and 1206.

Application Schematic

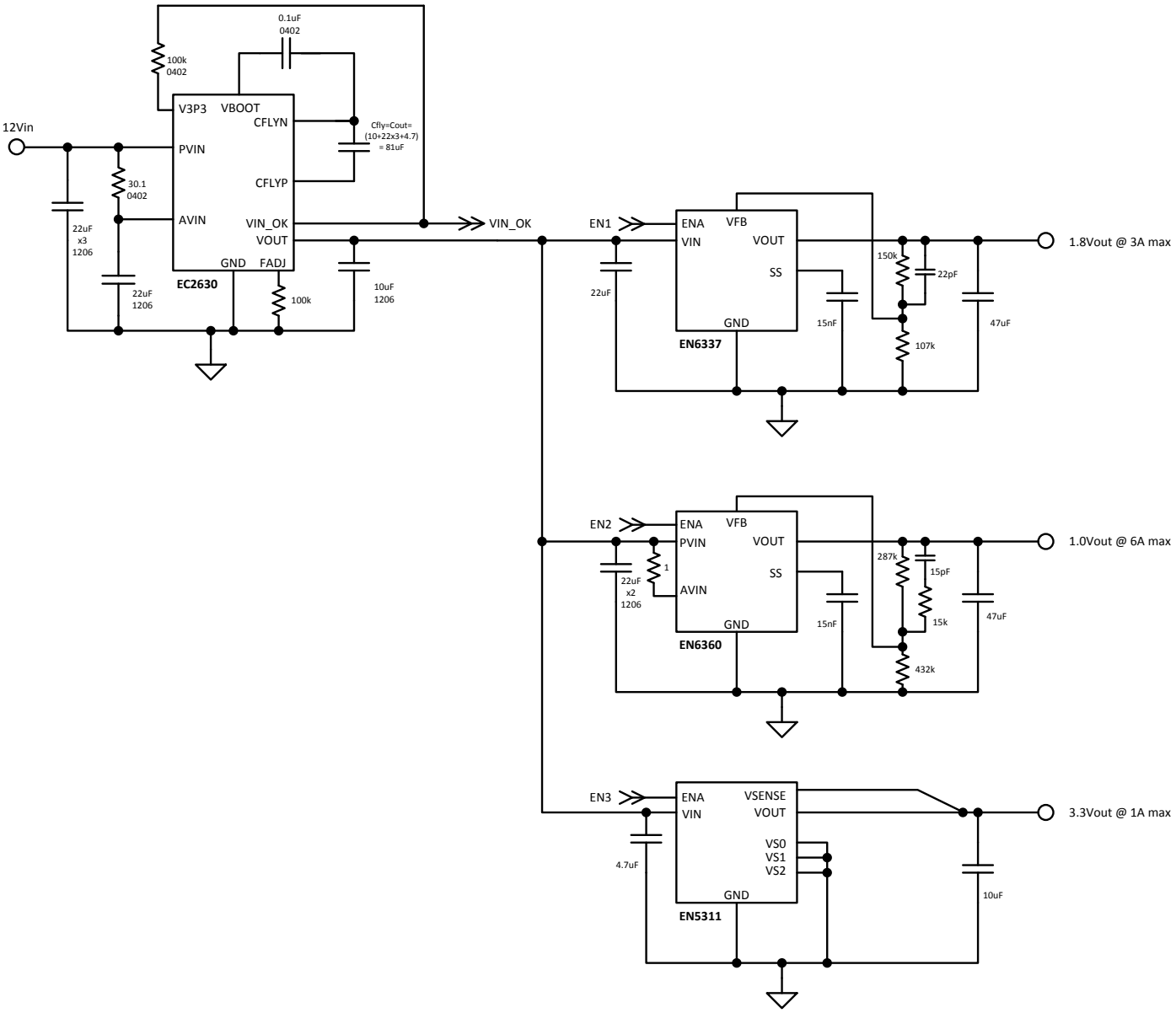


Figure 6. EC2630 connected to a 12V input supply supplying 3 point-**o**f-load Altera Enpirion DC-DC switchers

Figure 6 shows a typical application where the EC2630 is powering up three downstream Altera Enpirion point-of-load (POL) converters. The EC2630 VIN_OK signal, along with a sequencer if necessary, is used to control the ENABLE pins of the downstream devices based on the application's sequencing requirements. The sequencing has to ensure that the intermediate bus voltage is up before the POL converters start switching. In addition, it is recommended to use only Altera's Enpirion POL converters rated for up to 6.6V input voltage operation as downstream devices.

NOTE: The V3P3 supply is meant to power only internal circuitry, apart from a pull-up resistor to VIN_OK. Altera recommends a 100kΩ pull-up resistor to V3P3 for most applications. Do not connect multiple pull-ups to the V3P3 pin.

Application Schematic

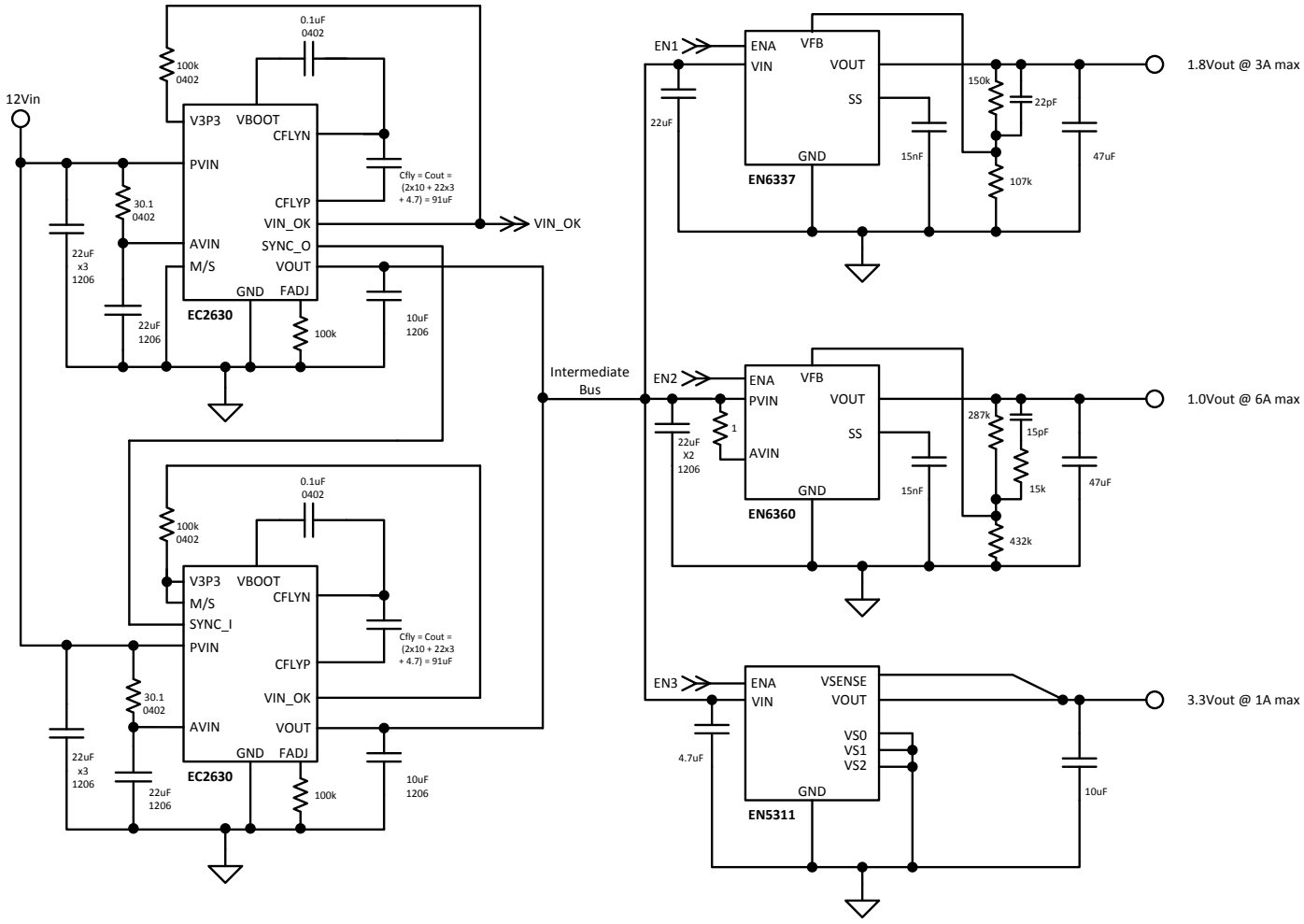


Figure 7. Parallel operation with two EC2630 devices

Figure 7 shows parallel operation of two EC2630 devices. The Master and Slave operate at a synchronized clock frequency, provided by the master through its SYNC_O pin. For parallel operation, no more than four parallel devices are recommended to ensure there are no significant voltage drops between the input supply and any of the paralleled devices.

Engineering Schematic

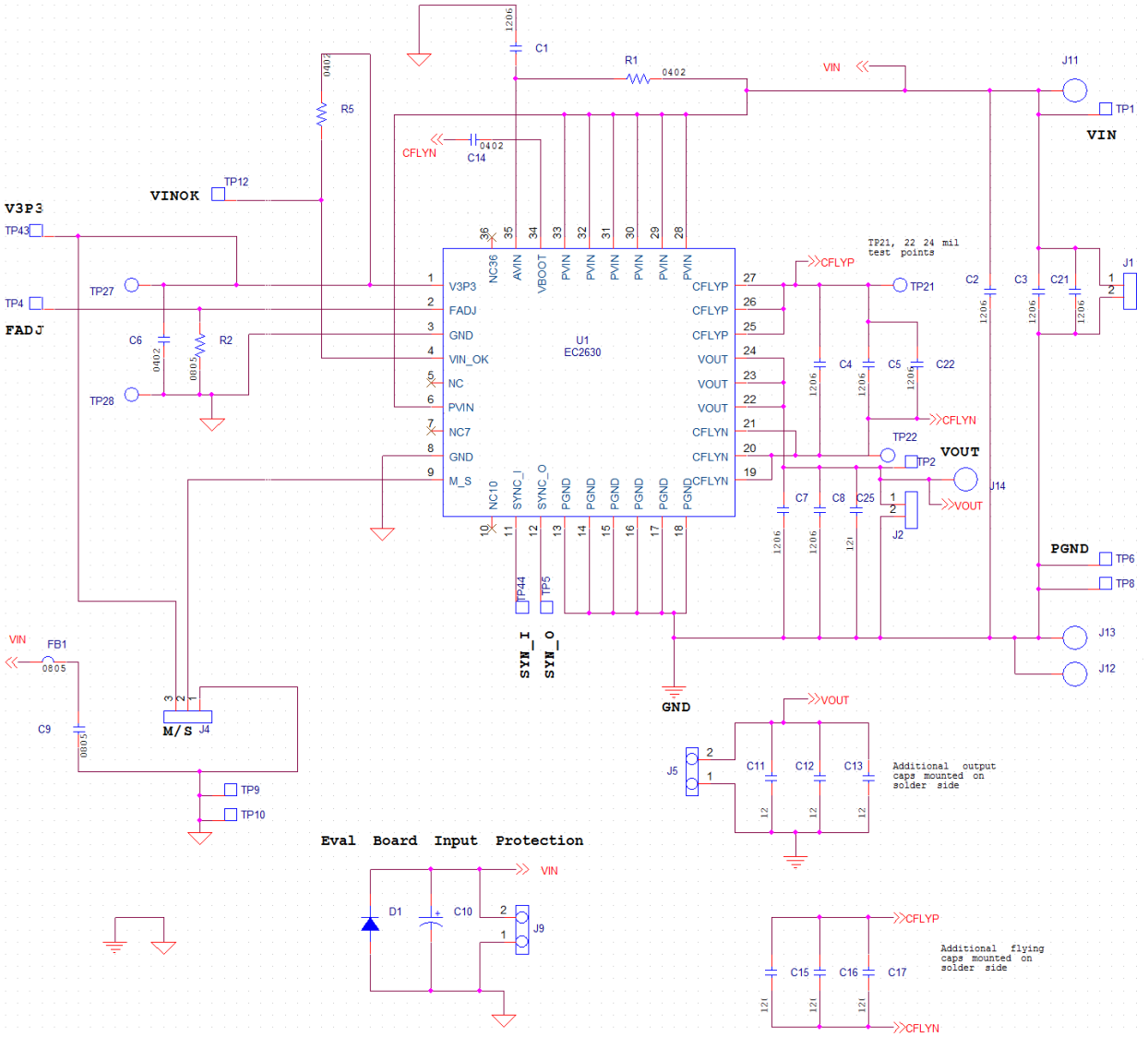


Figure 8. Engineering Schematic with Engineering Notes

Layout Recommendations

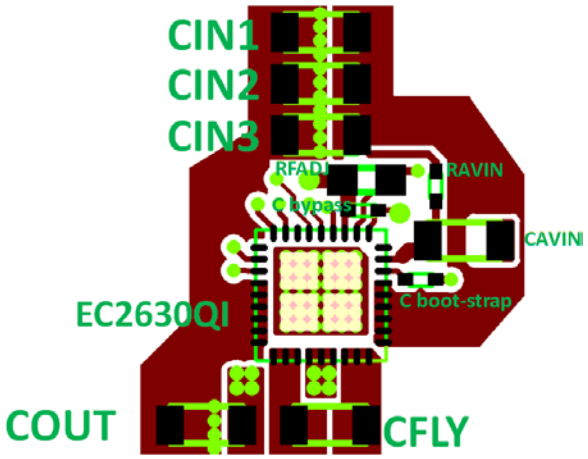


Figure 9. Top Layout with Critical Components Only (Top View). See Figure 8 for corresponding schematic

This layout only shows the critical components and top layer traces for minimum footprint. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at www.altera.com/enpirion for details on all layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EC2630QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EC2630QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 8 this connection is made at the input capacitor.

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Recommendation 7: Follow all the layout recommendations as close as possible to optimize performance. Not following layout recommendations can complicate designs and create anomalies different than the expected operation of the product.

Package and Mechanical

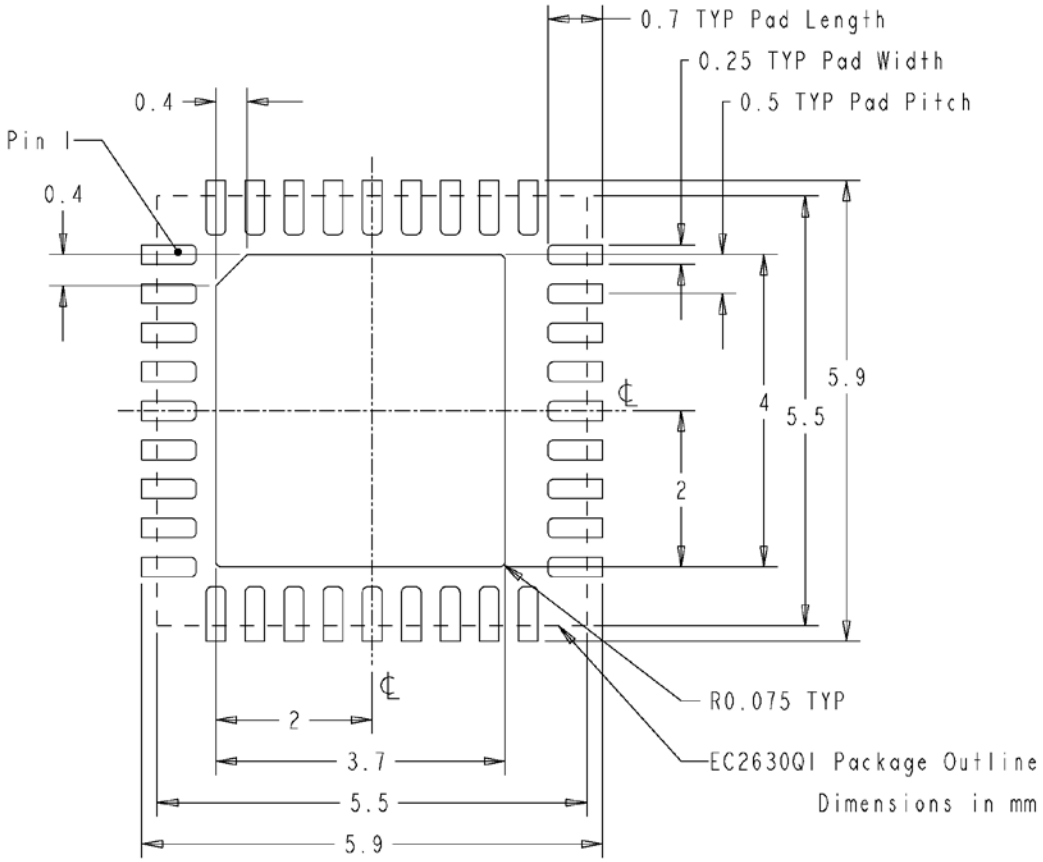

Figure 10. Recommended PCB footprint

Mechanical Information

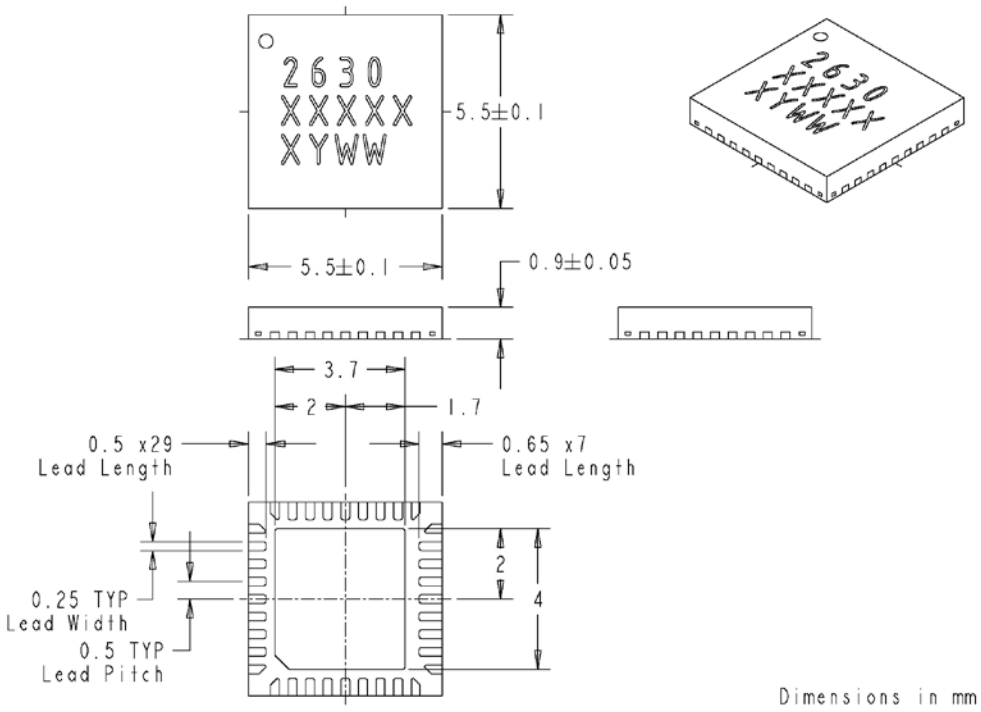

Figure 11. EC2630 Package Dimensions

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Revision History

Rev	Date	Change(s)
A	July 2011	• Introductory production datasheet
B	Sep 2013	• Formatting changes
C	May 2016	• Added solution size • Modified description of SYNC_O pin (removed frequency scaling) • Modified description of VBOOT pin (added Cboot recommendation) • VOUT_OK pin changed to NC. VIN_OK is used for sequencing downstream parts • ENABLE pin changed to PVIN (ensures part is always enable when powered) • VIN range changed to 10V - 13.2V with typ at 12. • Added VOUT min and max limits (as a percentage of Vin) • Added data on VIN_OK threshold limits • Added more characteristic curves (Vout vs Iout at various Vin, ripple, transients, parallel current share, etc) • Modified discussion on Frequency sync. • Added curves relating Cout/Cfly ratio to Outptut voltage over load and frequency • Modified application diagram to remove ENABLE, and modified ENABLE connections of downstream devices • Added VIN_OK pull-up resistor recommendation • Added application schematic and note on parallel operation • Added note to say that only Enpirion PoLs should be used for downstream devices and only other EC2630Qis should be used as parallel devices. • Removed external circuitry recommendations for OCP • Removed note to contact applications for support • Overall formatting changes to the document

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