

N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16323Q3](#)

FEATURES

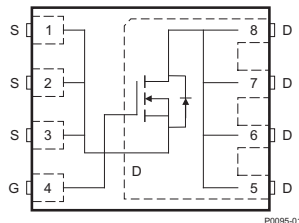
- Optimized for 5V Gate Drive
- Ultra Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

Top View


P0085-01

PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	25	V
Q _g	Gate Charge Total (4.5V)	6.2	nC
Q _{gd}	Gate Charge Gate to Drain	1.1	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V	5.4 mΩ
		V _{GS} = 4.5V	4.4 mΩ
		V _{GS} = 8V	3.8 mΩ
V _{th}	Threshold Voltage	1.1	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16323Q3	SON 3.3 × 3.3 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	25	V
V _{GS}	Gate to Source Voltage	+10 / -8	V
I _D	Continuous Drain Current, T _C = 25°C	60	A
	Continuous Drain Current ⁽¹⁾	21	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	112	A
P _D	Power Dissipation ⁽¹⁾	3	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I _D = 50A, L = 0.1mH, R _G = 25Ω	125	mJ

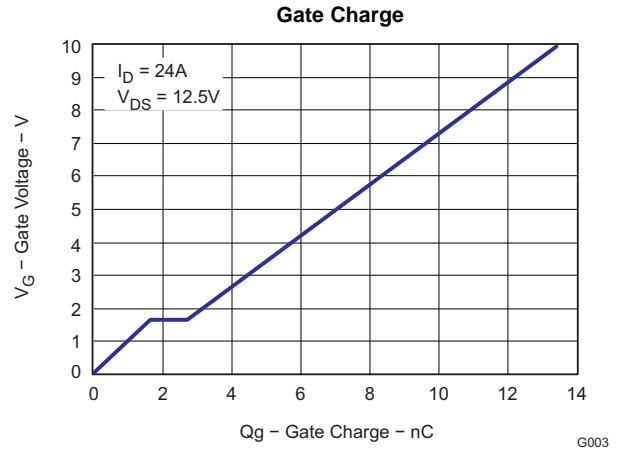
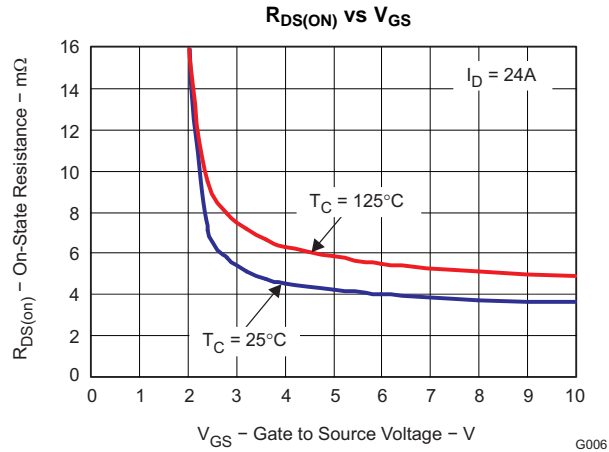
(1) R_{θJA} = 43°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ C$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V	
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA	
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA	
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.1	1.4	V	
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 24A$		5.4	7.2	m Ω	
		$V_{GS} = 4.5V, I_D = 24A$		4.4	5.5	m Ω	
		$V_{GS} = 8V, I_D = 24A$		3.8	4.5	m Ω	
g_{fs}	Transconductance	$V_{DS} = 12.5V, I_D = 24A$		108		S	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		1020	1300	pF	
C_{OSS}	Output Capacitance			740	960	pF	
C_{RSS}	Reverse Transfer Capacitance			50	65	pF	
R_g	Series Gate Resistance	$V_{DS} = 12.5V, I_D = 24A$		1.4	2.8	Ω	
Q_g	Gate Charge Total (4.5V)			6.2	8.4	nC	
Q_{gd}	Gate Charge Gate to Drain			1.1		nC	
Q_{gs}	Gate Charge Gate to Source			1.8		nC	
$Q_{g(th)}$	Gate Charge at V_{th}			1		nC	
Q_{OSS}	Output Charge		$V_{DS} = 12.5V, V_{GS} = 0V$		14		nC
$t_{d(on)}$	Turn On Delay Time		$V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 24A$ $R_G = 2\Omega$		5.3		ns
t_r	Rise Time			15		ns	
$t_{d(off)}$	Turn Off Delay Time			13		ns	
t_f	Fall Time			6.3		ns	
Diode Characteristics							
V_{SD}	Diode Forward Voltage	$I_S = 24A, V_{GS} = 0V$		0.85	1	V	
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/\mu s$		21		nC	
t_{rr}	Reverse Recovery Time	$V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/\mu s$		16		ns	

THERMAL INFORMATION

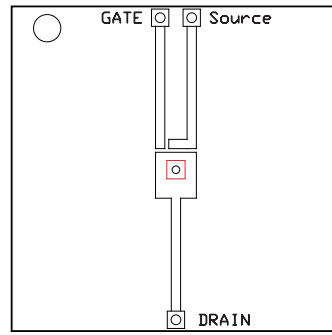
THERMAL METRIC ⁽¹⁾⁽²⁾		CSD16323Q3	UNITS
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	42.0	°C/W
θ_{JcTop}	Junction-to-case (top) thermal resistance	20.6	
θ_{JB}	Junction-to-board thermal resistance	8.8	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	8.7	
θ_{JcBot}	Junction-to-case (bottom) thermal resistance	0.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
 (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



M0161-01

Max $R_{\theta JA} = 58^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.

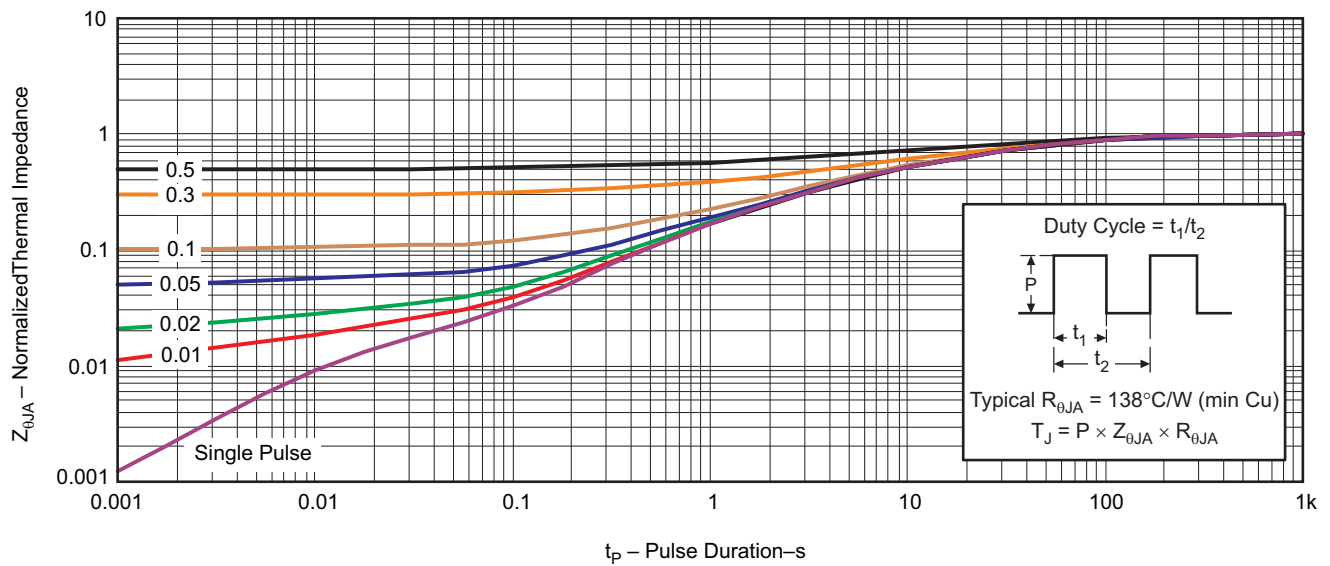


M0161-02

Max $R_{\theta JA} = 162^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

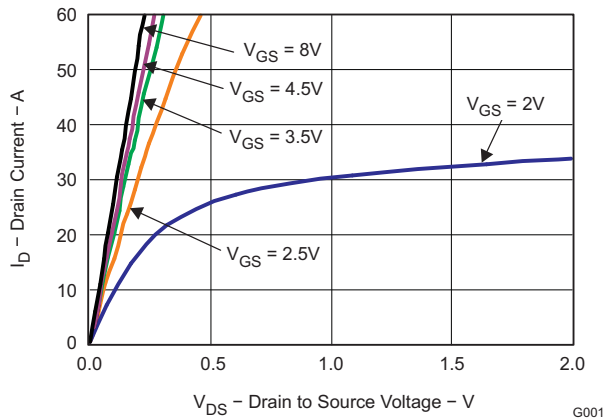


Figure 2. Saturation Characteristics

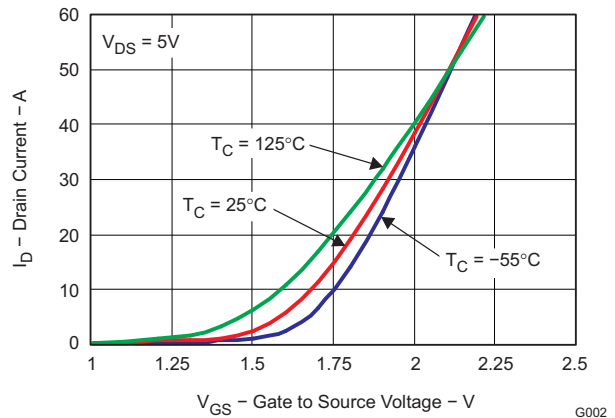


Figure 3. Transfer Characteristics

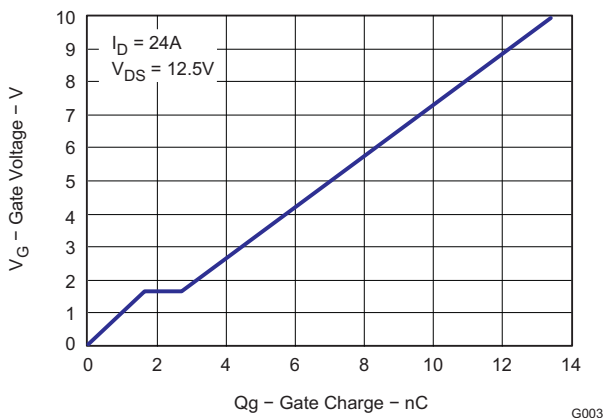


Figure 4. Gate Charge

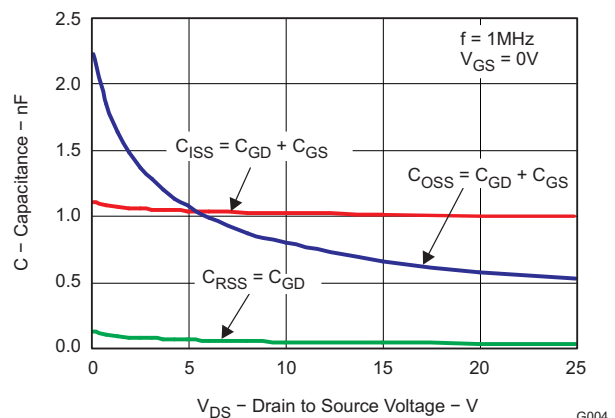


Figure 5. Capacitance

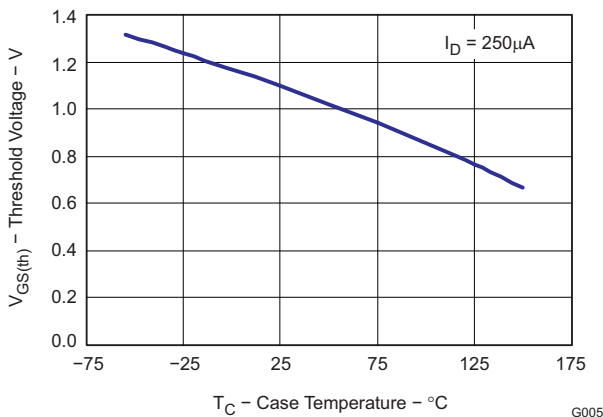


Figure 6. Threshold Voltage vs. Temperature

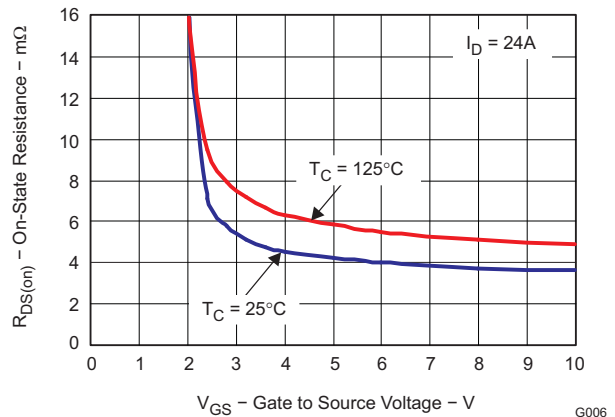


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

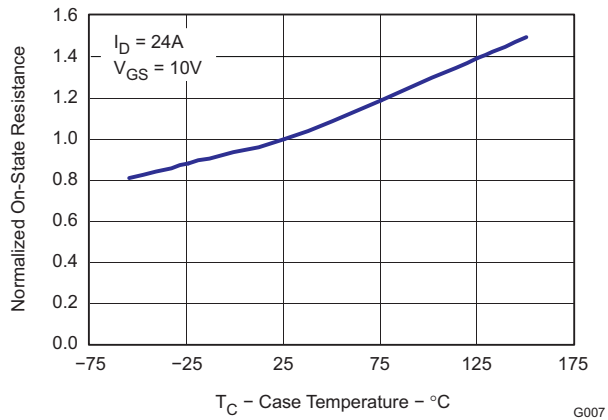


Figure 8. Normalized On Resistance vs. Temperature

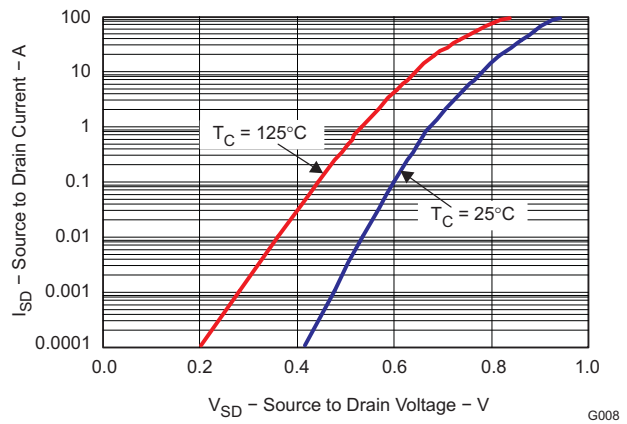


Figure 9. Typical Diode Forward Voltage

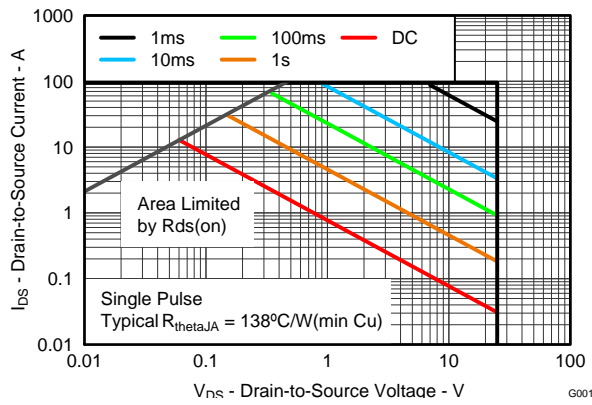


Figure 10. Maximum Safe Operating Area

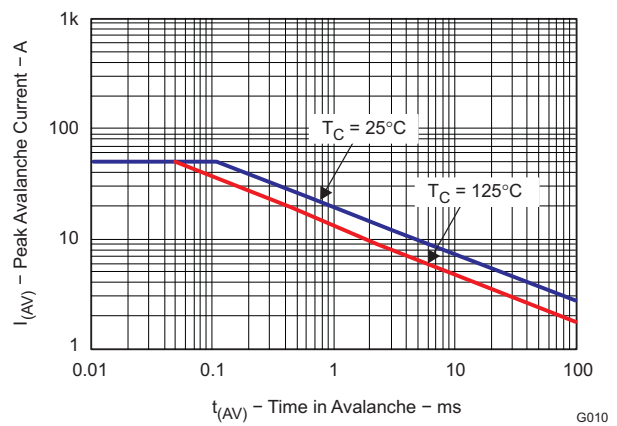


Figure 11. Single Pulse Unclamped Inductive Switching

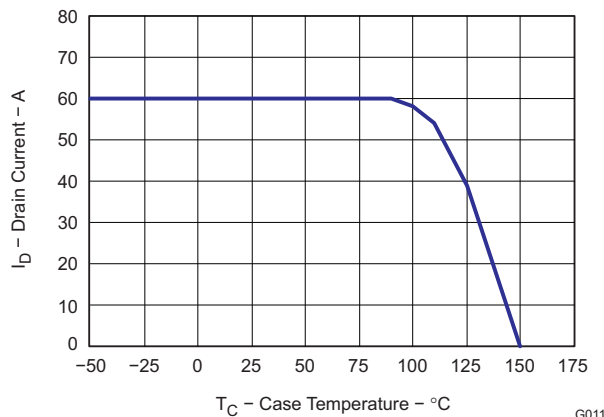
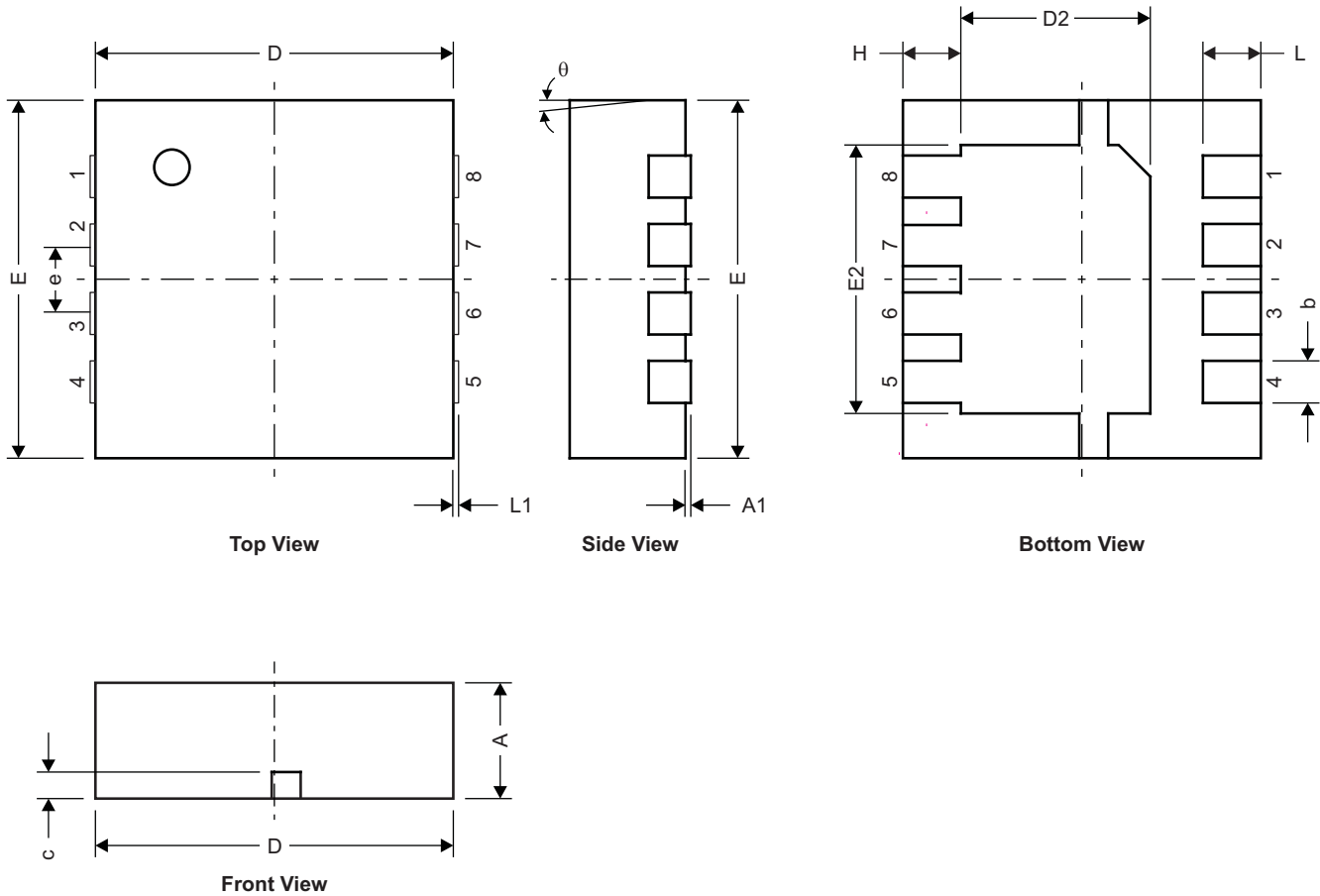


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

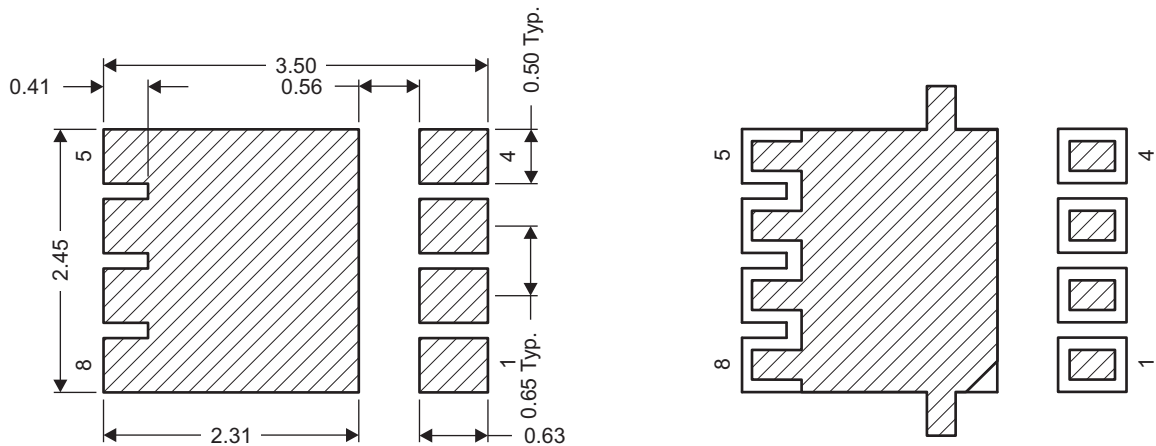
Q3 Package Dimensions



M0142-01

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	-	-	-
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	-	-	-	-
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	-
theta	-	-	-	-	-	-

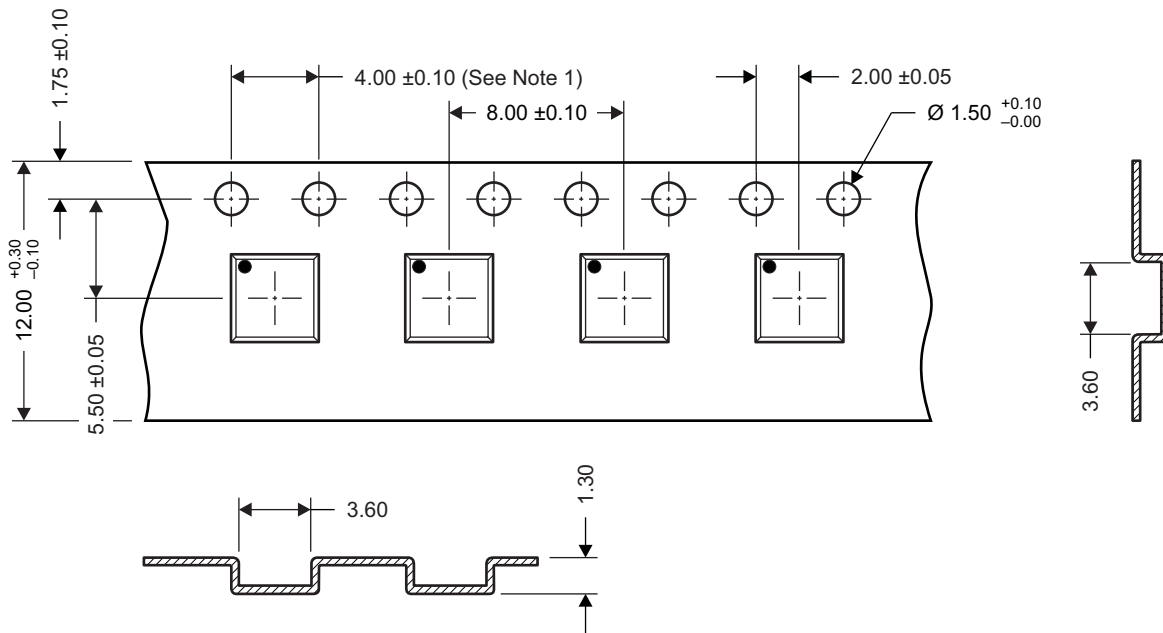
Recommended PCB Pattern



M0143-01

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A **Page**

- Changed $R_{DS(on)}$ - $V_{GS} = 3V$, $I_D = 24A$ MAX value From: 6.5 To: 7.2 **2**
 - Deleted the Package Marking Information section **8**
-

Changes from Revision A (April 2010) to Revision B **Page**

- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table **3**
 - Replaced [Figure 10](#) - Maximum Safe Operating Area **6**
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16323Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16323	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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